Publication List
Prof. Dr.-Ing. Jürgen Teich
(2005-2011)

Books, Monographs and Book Chapters

409 D. Ziener, M. Schmid and J. Teich.
Robustness Analysis of Watermark Verification Techniques for FPGA Netlist Cores.
Design Methodologies for Secure Embedded Systems, LNEE 78, pp. 105-127, Springer-Verlag, Heidelberg, 2010.

406 J. Falk, J. Keinert, C. Haubelt, J. Teich and C. Zebelein.
Integrated Modeling Using Finite State Machines and Dataflow Graphs.
In Handbook of Signal Processing Systems, pp. 1041-1075, Springer, 2010.

402 M. Streubühr, J. Gladigau, C. Haubelt and J. Teich.
Efficient Approximately-Timed Performance Modeling for Architectural Exploration of MPSoCs.
In D. Borrione editor, *Advances in Design Methods from Modeling Languages for Embedded Systems and SoC's*, volume 63 of *Lecture Notes in Electrical Engineering*. pp. 59-72, Springer Netherlands, 2010.

399 C. Haubelt and J. Teich.
Digitale Hardware/Software-Systeme: Spezifikation und Verifikation.
1. Auflage, Springer-Verlag, Berlin, Heidelberg, Germany, 2010.

378 S. Fekete, T. Kamphans, N. Schweer, C. Tessars, J. van der Veen, A. Ahmadinia, J. Angermeier, D. Koch, M. Majer and J. Teich.
ReCoNodes - Optimization Methods for Module Scheduling and Placement on Reconfigurable Hardware Devices.
In Dynamically Reconfigurable Systems - Architectures, Design Methods and Applications, p. 199-222, Springer, Heidelberg, February 2010.

377 D. Koch, T. Streichert, C. Haubelt, F. Reimann and J. Teich.
ReCoNets – Design Methodology for Embedded Systems Consisting of Small Networks of Reconfigurable Nodes and Connections.
In Dynamically Reconfigurable Systems - Architectures, Design Methods and Applications, p. 223-244, Springer, Heidelberg, February 2010

376 M. Platzner, J. Teich and N. Wehn.
Dynamically Reconfigurable Systems - Architectures, Design Methods and Applications.
Springer, Heidelberg, February 2010.

375 J. Angermeier, C. Bobda, M. Majer and J. Teich.
Erlangen Slot Machine: An FPGA-Based Dynamically Reconfigurable Computing Platform.
In Dynamically Reconfigurable Systems - Architectures, Design Methods and Applications, p. 51-71, Springer, Heidelberg, February 2010.

351 J. Gladigau, C. Haubelt and J. Teich.
Symbolic Scheduling of SystemC Dataflow Designs.
In M. Radetzki, editor, *Languages for Embedded Systems and their Applications*, Volume 36 of *Lecture Notes in Electrical Engineering*, pages 183–199. Springer Netherlands, 2009.

291 A. Kupriyanov, F. Hannig, D. Kissler and J. Teich.
MAML: An ADL for Designing Single and Multiprocessor Architectures.
In Processor Description Languages - Applications and Methodologies, Prabhat Mishra and Nikil Dutt, eds., pages 295-327, Morgan Kaufmann, 2008.

276 T. Streichert, C. Haubelt, D. Koch and J. Teich.
Concepts for Self-Adaptive and Self-Healing Networked Embedded Systems.
Organic Computing, Rolf Würtz (Ed.), Springer Series Understanding Complex Systems, pp. 241-260, Springer, 2008.

258 B. Niemann, C. Haubelt, M. Uribe and J. Teich.
Formalizing TLM with Communicating State Machines.
In Advances in Design and Specification Languages for Embedded Systems, Sorin Huss (Ed.), pp. 225-242, Springer, 2007.

260 J. Teich.
Reconfigurable Computing Systems.
it - Information Technology, http://it-information-technology.de, Oldenbourg Wissenschaftsverlag, vol. 49(3):139-142, 2007.

239 J. Teich and C. Haubelt.
Digitale Hardware/Software-Systeme: Synthese und Optimierung.
2. Auflage, Springer-Verlag, Berlin Heidelberg, 2007.

236 C. Haubelt and J. Teich.
Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen.
Shaker Verlag, Aachen, Germany, 2007.

175 S. Mostaghim and J. Teich.
Quad-trees: A Data structure for storing Pareto-sets in Multi-objective Evolutionary Algorithms with Elitism.
In Ajith Abraham and Lakhmi Jain and Robert Goldberg (eds.), Evolutionary Multiobjective Optimization, Theoretical Advances and Applications. Springer Advanced Information and Knowledge Processing Series, London, pp. 81-104, 2005.

Reviewed Journal Articles

447 D. Kissler, D. Gran, Z. Salcic, F. Hannig and J. Teich.
Scalable Many-Domain Power Gating in Coarse-grained Reconfigurable Processor Arrays.
IEEE Embedded Systems Letters, to appear.

441 T. Ziermann, S. Wildermann and J. Teich.
OrganicBus: Organic Self-organising Bus-Based Communication Systems.
In Organic Computing - A Paradigm Shift for Complex Systems, pp. 489-501, Birkhäuser Verlag, 2011.

435 R. Membarth, H. Dutta, F. Hannig and J. Teich.
Efficient Mapping of Streaming Applications for Image Processing on Graphics Cards.
Transactions on High-Performance Embedded Architectures and Compilers (Transactions on HiPEAC), 5(3), 2011.

430 T. Ziermann, S. Wildermann and J. Teich.
Distributed Self-organizing Bandwidth Allocation for Priority-based Bus Communication.
In Concurrency and Computation: Practice and Experience, Wiley Online Library, 2011.

423 J. Keinert and J. Teich.
Design of Image Processing Embedded Systems Using Multidimensional Data Flow.
Series Embedded Systems, Springer, New York, 1st edition, 2011.

418 D. Kissler, F. Hannig and J. Teich.
Efficient Evaluation of Power/Area/Latency Design Trade-offs for Coarse-Grained Reconfigurable Processor Arrays.
Journal of Low Power Electronics, American Scientific Publishers, 2011, to appear.

417 J. Teich, J. Henkel, A. Herkersdorf, D. Schmitt-Landsiedel, W. Schröder-Preikschat and G. Snelting.
Invasive Computing: An Overview.
In Multiprocessor System-on-Chip, M. Hübner and J. Becker (Eds.), Chapter 11, pages 241-268, Springer, 2011.

415 R. Membarth, H. Dutta, F. Hannig and J. Teich.
Efficient Mapping of Streaming Applications for Image Processing on Graphics Cards.
To appear in Transactions on High-Performance Embedded Architectures and Compilers (Transactions on HiPEAC), 2010.

365 A. Gerstlauer, C. Haubelt, A. Pimentel, T. Stefanov, D. Gajski and J. Teich.
Electronic System-Level Synthesis Methodologies.
IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 28(10), pages 1517-1530, October 2009.

355 D. Ziener and J. Teich.
Concepts for run-time and error-resilient control flow checking of embedded RISC CPUs.
Int. Journal of Autonomous and Adaptive Communications Systems, Vol. 2, No. 3, pages 256-275, Inderscience Enterprises Ltd, 2009.

330 D. Kissler, A. Strawetz, F. Hannig and J. Teich.
Power-efficient Reconfiguration Control in Coarse-grained Dynamically

Reconfigurable Architectures.
Journal of Low Power Electronics, 5(1):96-105, American Scientific Publishers, 2009.

329 H. Dutta, D. Kissler, F. Hannig, A. Kupriyanov, J. Teich and B. Pottier.
A Holistic Approach for Tightly Coupled Reconfigurable Parallel Processors.
Microprocessors and Microsystems, 33(1):53-62, 2009.

328 J. Keinert, M. Streubühr, T. Schlichter, J. Falk, J. Gladigau, C. Haubelt, J. Teich and M. Meredith.
SYSTEMCODESIGNER - An Automatic ESL Synthesis Approach by Design Space Exploration and Behavioral Synthesis for Streaming Applications.
ACM Transactions on Design Automation of Electronic Systems, 14(1), pp. 1-23, 2009.

326 D. Koch, C. Beckhoff and J. Teich.
Hardware Decompression Techniques for FPGA-based Embedded Systems.
ACM Transactions on Reconfigurable Technology and Systems (TRETS), Vol.2, No. 9, June 2009.

318 J. Teich.
Invasive Algorithms and Architectures.
it - Information Technology, http://it-information-technology.de, Oldenbourg Wissenschaftsverlag, vol. 50(5):300-310, 2008.

313 S. Fekete, J. van der Veen, A. Ahmadinia, D. Göhringer, M. Majer and J. Teich.
Offline and Online Aspects of Defragmenting the Module Layout of a Partially Reconfigurable Device.
IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol.16(9):1210-1219, September 2008.

303 C. Haubelt, J. Teich and R. Dorsch.
Entdecke die Möglichkeiten.
In Design&Elektronik (8):22-27, 2008, WEKA.

286 D. Ziener and J. Teich.
Power Signature Watermarking of IP Cores for FPGAs .
Journal of VLSI Signal Processing Systems, Volume 51, Number 1 / April 2008, pages 123-136, Springer.

267 T. Streichert, M. Glaß, C. Haubelt and J. Teich.
Design space exploration of reliable networked embedded systems.
Journal on Systems Architecture (JSA). Vol. 53(10): 751-763, 2007.

253 H. Dutta, F. Hannig, H. Ruckdeschel and J. Teich.
Efficient Control Generation for Mapping Nested Loop Programs onto Processor Arrays.
Journal of Systems Architecture, Vol. 53(5-6):300-309, 2007.

250 D. Kissler, F. Hannig and J. Teich.
Schwach-programmiert macht stark.
Design&Elektronik, April 2007, pp. 34-39, WEKA Fachzeitschriften-Verlag GmbH.

247 T. Streichert, C. Strengert, D. Koch, C. Haubelt and J. Teich.
Communication Aware Optimization of the Task Binding in Hardware/Software Reconfigurable Networks.
Journal on Integrated Circuits and Systems, Vol. 2, No. 1, pp. 29-36, March 2007.

238 C. Haubelt, J. Falk, J. Keinert, T. Schlichter, M. Streubühr, A. Deyhle, A. Hadert and J. Teich.
A SystemC-based Design Methodology for Digital Signal Processing Systems.
EURASIP Journal on Embedded Systems, Special Issue on Embedded Digital Signal Processing Systems, Volume 2007 (2007), Article ID 47580, 22 pages, March 2007.

237 M. Majer, J. Teich, A. Ahmadinia and C. Bobda.
The Erlangen Slot Machine: A Dynamically Reconfigurable FPGA-Based Computer.
Journal of VLSI Signal Processing Systems, Springer, Vol. 47(1), pages 15-31, March 2007.

234 N. Bergmann, M. Platzner and J. Teich.
Dynamically Reconfigurable Architectures.
EURASIP Journal of Embedded Systems, Volume 2007 (2007), Article ID 28405, 2 pages, February 2007.

233 J. Angermeier, D. Göhringer, M. Majer, J. Teich, S. Fekete and J. van der Veen.
The Erlangen Slot Machine - A Platform for Interdisciplinary Research in Reconfigurable Computing.
it - Information Technology, http://it-information-technology.de, Oldenbourg Wissenschaftsverlag, Vol. 49(3):143-148, 2007.

231 A. Ahmadinia, C. Bobda, S. Fekete, J. Teich and J. van der Veen.
Optimal free-space management and routing-conscious dynamic placement for reconfigurable computing.
IEEE Transactions on Computers, Vol. 56, No. 3, pages 673-680, 2007.

224 T. Streichert, D. Koch, C. Haubelt and J. Teich.
Modeling and Design of Fault-Tolerant and Self-Adaptive Reconfigurable Networked Embedded Systems.
EURASIP Journal on Embedded Systems, Volume 2006 (2006), Article ID 42168, 15 pages, Hindawi Publishing Corporation.

215 S. Fekete, E. Köhler and J. Teich.
Higher-dimensional packing with order constraints.
SIAM Journal on Discrete Mathematics,Vol. 20, No. 4, pp. 1056-1078, 2006.

209 F. Hannig, H. Dutta and J. Teich.
Mapping a Class of Dependence Algorithms to Coarse-grained Reconfigurable Arrays: Architectural Parameters and Methodology.
International Journal of Embedded Systems, Vol. 2, Nos. 1/2, pp. 114-127, 2006.

208 C. Haubelt, T. Schlichter and J. Teich.
Improving Automatic Design Space Exploration by Integrating Symbolic Techniques into Multi-Objective Evolutionary Algorithms.
International Journal of Computational Intelligence Research (IJCIR), Special Issue on Multiobjective Optimization and Applications, Volume 2, Issue 3. pp. 239-254, 2006.

207 J. Teich and S. Bhattacharyya.
Analysis of Dataflow Programs with Interval-limited Data-rates.
Journal of VLSI Signal Processing, Vol. 43, Nos. 2-3, pp. 247-258, 2006.

206 A. Ahmadinia, C. Bobda and J. Teich.
Online Placement for Dynamically Reconfigurable Devices.
Int. Journal of Embedded Systems, Vol. 1, Nos. 3/4, pp.165-178, 2006.

Reviewed Conference and Workshop Publications

446 S. Wildermann, D. Ziener and J. Teich.
Unifying Partitioning and Placement for SAT-based Exploration of Heterogeneous Reconfigurable SoCs.
Proceedings of the Conference on Field Programmable Logic and Applications 2011, Chania, Crete, GREECE, Sep. 5-7, 2011, to appear.

445 J. Angermeier, D. Ziener, M. Glaß and J. Teich.
Stress-Aware Module Placement on Reconfigurable Devices.
Proceedings of International Conference on Field-Programmable Logic and Applications (FPL 2011). Chania, Crete, Greece. September 2011, to appear.

444 J. Teich and D. Ziener.
Verifying the Authorship of Embedded IP Cores: Watermarking and Core Identification Techniques.
Proceedings of the International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA'11), Las Vegas, USA, July 18-21, 2011, to appear.

443 M. Lukasiewycz, M. Glaß, F. Reimann and J. Teich.
Opt4J - A Modular Framework for Meta-heuristic Optimization.
Proceedings of the Genetic and Evolutionary Computing Conference (GECCO 2011), Dublin, Ireland, July 12-16, 2011, to appear.

442 F. Hannig, S. Roloff, G. Snelting, J. Teich and A. Zwinkau.
Resource-Aware Programming and Simulation of MPSoC Architectures through Extension of X10.
Proceedings of the 14th International Workshop on Software and Compilers for Embedded Systems (SCOPES), St. Goar, Germany, June 27-28, 2011, to appear.

440 R. Kiesel, M. Streubühr, C. Haubelt, O. Löhlein and J. Teich.
Calibration and Validation of Software Performance Models for Pedestrian Detection Systems.
Proceedings of the International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation, July 2011, to appear.

439 A. Kern, H. Zhang, T. Streichert and J. Teich.
Testing Switched Ethernet Networks in Automotive Embedded Systems.
Proceedings of the International Symposium on Industrial Embedded Systems (SIES 2011), Västerås, Sweden, June 15-17, 2011.

438 F. Reimann, M. Lukasiewycz, M. Glaß, C. Haubelt and J. Teich.
Symbolic System Synthesis in the Presence of Stringent Real-Time Constraints.
Proceedings of the 48th Design Automation Conference (DAC 2011), San Diego, USA, June 5–10, 2011.

437 R. Membarth, F. Hannig, J. Teich, M. Körner and W. Eckert.
Frameworks for GPU Accelerators: A Comprehensive Evaluation using 2D/3D Image Registration.
Proceedings of the 9th IEEE Symposium on Application Specific Processors (SASP), San Diego, CA, USA, June 5-6, 2011 .

436 A. Kern, H. Zinner, T. Streichert, J. Nöbauer and J. Teich.
Accuracy of Ethernet AVB Time Synchronization Under Varying Temperature Conditions for Automotive Networks.
Proceedings of the 48th Design Automation Conference (DAC 2011), San Diego, USA, June 5–10, 2011.

434 P. Kutzer, J. Gladigau, C. Haubelt and J. Teich.
Automatic Generation of System-Level Virtual Prototypes from Streaming Application Models.
Proceedings of the 22nd IEEE International Symposium on Rapid System Prototyping, Karlsruhe, Germany, May 24-27, 2011.

433 V. Lari, F. Hannig and J. Teich.
Distributed Resource Reservation in Massively Parallel Processor Arrays.
In Proceedings of 18th Reconfigurable Architectures Workshop (RAW 2010), International Symposium on Parallel and Distributed Processing Symposium (IPDPS) 2011, Anchorage, USA, May 2011 (to appear)..

432 S. Graf, M. Streubühr, M. Glaß and J. Teich.
Analyzing Automotive Networks using Virtual Prototypes.
In Proceedings of Automotive meets Electronics (AmE 2011), pp. 10-15, Dortmund, Germany, May 4-5, 2011.

431 A. Weichslgartner, S. Wildermann and J. Teich.
Dynamic Decentralized Mapping of Tree-Structured Applications on NoC Architectures.
In Proceedings of the Fifth ACM/IEEE International Symposium on Networks-on-Chip (NOCS 2011), Pittsburgh, USA, May 1-4, 2011.

428 J. Angermeier, E. Sibirko, R. Wanka and J. Teich.
Bitonic Sorting on Dynamically Reconfigurable Architectures.
Proceedings of 18th Reconfigurable Architectures Workshop (RAW 2010), International Symposium on Parallel and Distributed Processing Symposium (IPDPS) 2011, Anchorage, USA, May 2011..

427 A. Kern, T. Streichert and J. Teich.
An Automated Data Structure Migration Concept - From CAN to Ethernet/IP in Automotive Embedded Systems (CANoverIP).
Proceedings of Design, Automation and Test in Europa (DATE'11), IEEE Computer Society, Grenoble, France, March 14-18, 2011.

426 T. Ziermann, Z. Salcic and J. Teich.
DynOAA - Dynamic Offset Adaptation Algorithm for Improving Response Times of CAN Systems.
Proceedings of Design, Automation and Test in Europe (DATE'11), IEEE Computer Society, Grenoble, France, March 14-18, 2011.

425 J. Falk, C. Zebelein, C. Haubelt and J. Teich.
A Rule-Based Static Dataflow Clustering Algorithm for Efficient Embedded Software Synthesis.
Proceedings of Design, Automation and Test in Europe (DATE'11), IEEE Computer Society, Grenoble, France, March 14-18, 2011.

424 P. Kutzer, M. Streubühr, C. Haubelt, J. Teich and A. von Schwerin.
Actor-oriented Modeling of Industrial Ethernet in the Automation Domain Using SystemC .
Proceedings of the Embedded World Conference, Nuremberg, Germany, March 01-03, 2011.

422 N. Mühleis, M. Glaß and J. Teich.
Control Performance-Aware System Level Design.
In Proceedings of the 8th Workshop on Cyber-Physical Systems – Enabling Multi-Nature Systems (CPMNS 2011), pp. 15-20, Bremen, Germany, February 23-24, 2011.

421 A. Kern, D. Reinhard, T. Streichert and J. Teich.
Gateway Strategies for Embedding of Automotive CAN-frames into Ethernet-packets and Vice Versa.
Proceedings of Architecture of Computing Systems Conference (ARCS'11), Lake Como, Italia, Feb 22-25, 2011..

420 R. Membarth, F. Hannig, J. Teich, M. Körner and W. Eckert.
Frameworks for Multi-core Architectures: A Comprehensive Evaluation using 2D/3D Image Registration.
Proceedings of the 24th International Conference on Architecture of Computing Systems (ARCS), pp. 62-73, Lake Como, Italy, February 22-25, 2011.

419 R. Membarth, F. Hannig, J. Teich, G. Litz and H. Hornegger.
Detector Defect Correction of Medical Images on Graphics Processors.
Proceedings of the SPIE: Medical Imaging 2011: Image Processing, pp. 79624M 1-12, Lake Buena Vista, Orlando, FL, USA, February 12-17, 2011.

414 J. Angermeier, S. Wildermann, E. Sibirko and J. Teich.
Placing Streaming Applications with Similarities on Dynamically Partially Reconfigurable Architectures.

To appear in Proceedings of International Conference on ReConFigurable Computing and FPGAs, December 13-15, 2010, Cancun, Mexico.

413 F. Hannig, M. Schmid, J. Teich and H. Hornegger.
A Deeply Pipelined and Parallel Architecture for Denoising Medical Images.
To appear in Proceedings of the IEEE International Conference on Field Programmable Technology (FPT), Beijing, China, December 8-10, 2010.

412 M. Glaß, M. Lukasiewycz, F. Reimann, C. Haubelt and J. Teich.
Symbolic System Level Reliability Analysis.
To appear in Proceedings of the International Conference on Computer-Aided Design (ICCAD), San Jose, USA. November 07-11 2010.

411 S. Wildermann, A. Oetken, J. Teich and Z. Salcic.
Self-Organizing Computer Vision for Robust Object Tracking in Smart Cameras.
To appear in Proceedings of 7th International Conference on Autonomic and Trusted Computing, Xi'an, China. October 26-29, 2010.

410 F. Reimann, M. Glaß, C. Haubelt, M. Eberl and J. Teich.
Improving Platform-Based System Synthesis by Satisfiability Modulo Theories Solving.
Proceedings of the 8th International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS), Scottsdale, USA, October 24-29 2010.

407 A. Oetken, S. Wildermann, J. Teich and D. Koch.
A Bus-based SoC Architecture for Flexible Module Placement on Reconfigurable FPGAs.
In Proceedings of the International Conference on Field Programmable Logic and Applications (FPL), Milan, Italy, Aug. 31st - Sep. 2nd, 2010.

403 A. Kern, C. Schmutzler, T. Streichert, M. Hübner and J. Teich.
Network Bandwidth Optimization of Ethernet-based Streaming Applications in Automotive Embedded Systems.
In Proceedings of the International Conference on Computer Communication Networks (ICCCN) 2010 – Track on Network Algorithms, Performance Evaluation and Theory (NAPET), Zurich, Switzerland, August 2-5, 2010.

401 J. Gladigau, A. Gerstlauer, M. Streubühr, C. Haubelt and J. Teich.
A System-Level Synthesis Approach from Formal Application Models to Generic Bus-Based MPSoCs.
Proceedings of the International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS), pp.118-125, Samos, Greece, July 19-22, 2010.

397 D. Ziener, F. Baueregger and J. Teich.
Multiplexing Methods for Power Watermarking.
In Proceedings of the IEEE Int. Symposium on Hardware-Oriented Security and Trust (HOST 2010), pp. 54-59, Anaheim, CA, USA, June 13-14, 2010.

396 M. Glaß, M. Lukasiewycz, C. Haubelt and J. Teich.
Towards Scalable System-Level Reliability Analysis.

In Proceedings of the 2010 ACM/EDAC/IEEE Design Automation Conference (DAC 2010), pp. 234-239, Anaheim, CA, USA, June 13-18, 2010.

395 T. Ziermann, N. Mühleis, S. Wildermann and J. Teich.
Self-organizing Distributed Reinforcement Learning Algorithm to Achieve Fair Bandwidth Allocation for Priority-based Bus Communication.
In Proceedings of the 1st IEEE Workshop on Self-Organizing Real-Time systems (SORT 2010), Camora, Spain, pp. 11-20, May 2010. Invited Paper.

394 J. Sim, W. Wong, G. Walla, T. Ziermann and J. Teich.
Interprocedural Placement-Aware Configuration Prefetching for FPGA-based Systems.
In Proceedings of the 18th Annual International IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM'10), Charlotte, USA, pp. 179 - 182, May 02-04, 2010, HiPEAC Award.

393 D. Ziener, F. Baueregger and J. Teich.
Using the Power Side Channel of FPGAs for Communication.
In Proceedings of the 18th Annual International IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM'10), Charlotte, USA, May 02-04, pp. 237-244, 2010.

392 J. Angermeier, J. Teich, T. Kamphans and S. Fekete.
Virtual Area Management: Multitasking on Dynamically Partially Reconfigurable Devices.
In Proceedings of 17th Reconfigurable Architectures Workshop (RAW 2010), Atlanta, USA, April 19-20, 2010.

391 T. Ziermann and J. Teich.
Adaptive Traffic Scheduling Techniques for Mixed Real-Time and Streaming Applications on Reconfigurable Hardware.
In Proceedings of 17th Reconfigurable Architectures Workshop (RAW), Atlanta, USA, April 19-20, 2010.

389 F. Reimann, A. Kern, C. Haubelt, T. Streichert and J. Teich.
Echtzeitanalyse Ethernet-basierter E/E-Architekturen im Automobil.
In: GMM-Fachbericht -- Automotive meets Electronics (AmE 2010), (64), p. 9–14, 2010,.

388 T. Ziermann and J. Teich.
Electromagnetic Compatibility (EMC) of CAN+.
Proceedings of Automotive meets Electronics (AmE 2010), pp. 25-30, Dortmund, Germany, April 15-16, 2010.

385 M. May, N. Wehn, A. Bouajila, J. Zeppenfeld, W. Stechele, A. Herkersdorf, D. Ziener and J. Teich.
A Rapid Prototyping System for Error-Resilient Multi-Processor Systems-on-Chip.
Proceedings of Design, Automation and Test in Europe (DATE'10), pp. 375-380, Dresden, Germany, March 08-12, 2010.

384 C. Zebelein, J. Falk, C. Haubelt, J. Teich and R. Dorsch.
Efficient High-Level Modeling in the Networking Domain.
Proceedings of Design, Automation and Test in Europe (DATE 2010), pp. 1189-1194, Dresden, Germany, March 8-12, 2010.

383 M. Lukasiewycz, M. Glaß and J. Teich.
Robust Design of Embedded Systems.
Proceedings of Design, Automation and Test in Europe (DATE 2010), pp. 1578-1583, Dresden, Germany, March 08-12, 2010.

382 M. Schmid, F. Hannig, J. Teich, R. Diefenbach, H. Pettendorf and H. Hornegger.
Discourse on Extending Embedded Medical Image Processing Systems Using the High Speed Serial RapidIO Interconnect.
Proceedings of the Embedded World Conference, Nuremberg, Germany, March 03-05, 2010.

381 R. Membarth, F. Hannig, J. Teich, M. Körner and W. Eckert.
Comparison of Parallelization Frameworks for Shared Memory Multi-Core Architectures.
Proceedings of the Embedded World Conference, Nuremberg, Germany, March 03-05, 2010.

380 J. Falk, C. Zebelein, C. Haubelt, J. Teich and R. Dorsch.
Integrating Hardware/Firmware Verification Efforts Using SystemC High-Level Models.
J. Falk, C. Zebelein, C. Haubelt, J. Teich and R. Dorsch Integrating Hardware/Firmware Verification Efforts Using SystemC High-Level Models. In 13. ITG/GI/GMM Workshop für Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen, pp. 137-146, Dresden, February 22-24, 2010.

379 R. Kiesel, O. Löhlein, A. Terzis, M. Streubühr, C. Haubelt and J. Teich.
Actor-oriented Modeling of Driver Assistance Systems for Efficient Multi-Core ECU Implementation.
In Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen, pages 117-126, Dresden, Germany, February 22-24, 2010.

374 M. Glaß, M. Lukasiewycz, C. Haubelt and J. Teich.
Lifetime Reliability Optimization for Embedded Systems: A System-Level Approach.
Proceedings of IEEE International Workshop on Reliability Aware System Design and Test (RASDAT '10), pp. 17-22, Bangalore, India, January 07-08, 2010.

372 S. Wildermann, T. Ziermann and J. Teich.
Run time Mapping of Adaptive Applications onto Homogeneous NoC-based Reconfigurable Architectures.
In Proceedings of the International Conference on Field-Programmable Technology (FPT'09), pp. 514-517, Sydney, Australia, December 9-11, 2009.

371 A. Amouri, F. Arifin, F. Hannig and J. Teich.

FPGA Implementation of an Invasive Computing Architecture.
In Proceedings of the International Conference on Field-Programmable Technology (FPT), pp. 135-142, Sydney, Australia, December 9-11, 2009.

370 J. Teich.
From Dynamic Reconfiguration to Self-Configuration: Invasive Algorithms and Architectures.
Proc. 2009 International Conference on Field-Programmable Technology (FPT'09), Sydney, Australia , pp. 11-12, December 9-11, 2009.

369 H. Greve, S. Egelkraut, M. Rösch, M. Glaß, M. März, J. Franke, J. Teich and L. Frey.
Zuverlässigkeitsuntersuchung von PBGA Lotverbindungen für Automobilanwendungen.
In Proceedings of IMAPS 2009, Munich, Germany, October 27-28, 2009.

368 F. Arifin, R. Membarth, A. Amouri, F. Hannig and J. Teich.
FSM-Controlled Architectures for Linear Invasion.
Proceedings of the 17th IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC), Florianópolis, Brazil, October 12-14, 2009.

367 M. Lukasiewycz, M. Glaß and J. Teich.
Exploiting Data-Redundancy in Reliability-Aware Networked Embedded System Design.
Proceedings of the 7th International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS), pp. 229-238, Grenoble, France, October 11-16, 2009.

366 M. Lukasiewycz, M. Glaß, P. Milbredt and J. Teich.
FlexRay Schedule Optimization of the Static Segment.
Proceedings of the 7th International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS), pp. 363-372, Grenoble, France, October 11-16, 2009.

364 M. Streubühr, J. Gladigau, C. Haubelt and J. Teich.
Efficient Approximately-Timed Performance Modeling for Architectural Exploration of MPSoCs.
Proceedings Forum on specification and Design Languages 2009, pp. 1-6, Sophia Antipolis, France, Sep. 22-24, 2009.

363 V. Lari, F. Hannig and J. Teich.
System Integration of Tightly-Coupled Reconfigurable Processor Arrays and Evaluation of Buffer Size Effects on Their Performance.
Proceedings of the 38th International Conference on Parallel Processing Workshops - the 4th International Symposium on Embedded Multicore Systems-on-Chip (MCSoC'09), pp. 528-534, Vienna, Austria, Sep. 22-25, 2009.

362 S. Wildermann, T. Ziermann and J. Teich.
Self-organizing Bandwidth Sharing in Priority-based Medium Access.
Proceedings of the Third IEEE International Conference on Self-Adaptive and Self-

Organizing Systems (SASO), pp.144-153, San Francisco, CA, USA, Sep. 14-18, 2009 .

361 S. Wildermann, G. Walla, T. Ziermann and J. Teich.
Self-Organizing Multi-cue Fusion for FPGA-based Embedded Imaging.
Proceedings of the International Conference on Field Programmable Logic and Applications (FPL), pp. 132 - 137, Prague, Czech Republic, Aug. 31 - Sep. 02, 2009.

360 M. Glaß, M. Lukasiewycz, J. Teich, U. Bordoloi and S. Chakraborty.
Designing Heterogeneous ECU Networks via Compact Architecture Encoding and Hybrid Timing Analysis.
Proceedings of the 2009 ACM/EDAC/IEEE Design Automation Conference (DAC 2009), pp. 43-46, San Francisco, CA, USA, July 26-31, 2009.

359 R. Membarth, F. Hannig, H. Dutta and J. Teich.
Efficient Mapping of Multiresolution Image Filtering Algorithms on Graphics Processors.
Proceedings of the 9th International Workshop on Systems, Architectures, Modeling, and Simulation (SAMOS Workshop), pp. 277-288, Samos, Greece, July 20-23, 2009.

358 R. Membarth, F. Hannig, H. Dutta and J. Teich.
Optimization Flow for Algorithm Mapping on Graphics Cards.
Proceedings of ACACES 2009 Poster Abstracts: Advanced Computer Architecture and Compilation for Embedded Systems, pp. 229-232, Barcelona, Spain, July 12-18, 2009.

356 R. Membarth, P. Kutzer, H. Dutta, F. Hannig and J. Teich.
Acceleration of Multiresolution Imaging Algorithms: A Comparative Study.
Proceedings of the 20th IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP), pp. 211-214, Boston, MA, USA, July 7-9, 2009.

352 J. Angermeier, A. Amouri and J. Teich.
General Methodology for Mapping Iterative Aproximation Algorithms to Adaptive Dynamically Partially Reconfigurable Systems.
Proceedings of International Conference on Field Programmable Logic and Applications (FPL), pp. 302-307, Prague, Czech Republic, August 31, 2009.

349 J. Keinert, C. Haubelt and J. Teich.
Data Flow Based System Level Design and Analysis of Concurrent Image Processing Applications.
Proceedings of DATE'09 Workshop on Designing for Embedded Parallel Computing Platforms: Architectures, Design Tools, and Applications, pp. 215-216, Nice, France, April 2009.

347 H. Dutta, J. Zhai, F. Hannig and J. Teich.
Impact of Loop Tiling on the Controller Logic of Hardware Acceleration Engines.
Proceedings of 20th IEEE International Conference on Application-specific Systems, Architectures, and Processors (ASAP), pp. 161-168, Boston, MA, USA, July 7-9, 2009.

346 J. Keinert, H. Dutta, F. Hannig, C. Haubelt and J. Teich.
Model-Based Synthesis and Optimization of Static Multi-Rate Image Processing Algorithms.
Proceedings of Design, Automation and Test in Europe (DATE 2009), pp. 135-140, IEEE Computer Society, Nice, France, April 20-24, 2009.

345 T. Ziermann, S. Wildermann and J. Teich.
CAN+: A New Backward-compatible Controller Area Network (CAN) Protocol with up to 16x Higher Data Rates.
Proceedings of Design, Automation and Test in Europe (DATE 2009), pp. 1088-1093, IEEE Computer Society, Nice, France, April 20-24, 2009.

344 M. Lukasiewycz, M. Streubühr, M. Glaß, C. Haubelt and J. Teich.
Combined System Synthesis and Communication Architecture Exploration for MPSoCs.
Proceedings of Design, Automation and Test in Europe (DATE 2009), pp. 472-477, IEEE Computer Society, Nice, France, April 20-24, 2009.

341 M. Glaß, M. Lukasiewycz, C. Haubelt and J. Teich.
Incorporating Graceful Degradation into Embedded System Design.
Proceedings of Design, Automation and Test in Europe (DATE 2009), pp. 320-323, IEEE Computer Society, Nice, France, April 20-24, 2009.

340 D. Koch, C. Beckhoff and J. Teich.
A Communication Architecture for Complex Runtime Reconfigurable Systems and its Implementation on Spartan-3 FPGAs.
Proceedings of the 17th ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA 2009), pp. 233-236, Monterey, CA, USA, February 22-24, 2009.

338 D. Koch, C. Beckhoff and J. Teich.
Minimizing Internal Fragmentation by Fine-grained Two-dimensional Module Placement for Runtime Reconfigurable Systems.
Proceedings 17th Annual IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM 2009), pp. 251-254, Napa, CA, USA, April 2009.

337 J. Sim, W. Wong and J. Teich.
Optimal Placement-aware Trace-based Scheduling of Hardware Reconfigurations for FPGA Accelerators.
Proceedings 17th Annual IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM 2009), pp. 279-282, Napa, CA, USA, April 2009.

335 T. Ziermann, J. Teich and S. Wildermann.
CAN+: Techniques and Prototype for Achieving Increased Data Rates on the Basis of Common CAN Bus Structures.
Proceedings of 9th Stuttgart International Symposium, pp. 327-339, Stuttgart, Germany, March 24-25, 2009 .

334 F. Hannig, H. Dutta and J. Teich.
Parallelization Approaches for Hardware Accelerators - Loop Unrolling versus Loop Partitioning.

In Proceedings of the 22nd International Conference on Architecture of Computing Systems (ARCS), pp. 16-27, Delft, The Netherlands, March 10-13, 2009.

333 H. Dutta, F. Hannig and J. Teich.
Performance Matching of Hardware Acceleration Engines for Heterogeneous MPSoC using Modular Performance Analysis.
In Proceedings of the 22nd International Conference on Architecture of Computing Systems (ARCS), pp. 233-245, Delft, The Netherlands, March 10-13, 2009.

332 M. Streubühr, M. Jäntsch, C. Haubelt and J. Teich.
From Model-based Design to Virtual Prototypes for Automotive Applications.
In Proceedings of the Embedded World Conference, pp. 1-10, Nuremberg, Germany, March 03-05, 2009.

331 J. Gladigau, C. Haubelt, M. Streubühr, J. Teich, A. Schneider, J. Knäblein and M. Lindig.
Testfallgenerierung für SystemC-Designs mit abstrakten Modellbeschreibungen.
In Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen, pages 157-166, Berlin, Germany, March 2-4, 2009.

327 M. Streubühr, C. Haubelt and J. Teich.
System Level Performance Simulation for Heterogeneous Multi-Processor Architectures.
1st HiPEAC Workshop on Rapid Simulation and Performance Evaluation: Methods and Tools (RAPIDO), in conjunction with the 4th HiPEAC Conference, pp. 47-52, Paphos, Cyprus, January 25, 2009.

324 M. Schmid, D. Ziener and J. Teich.
Netlist-Level IP Protection by Watermarking for LUT-Based FPGAs.
In Proceedings of IEEE International Conference on Field-Programmable Technology (FPT 2008), pp. 209-216, Taipei, Taiwan, December 08-10, 2008.

322 J. Falk, J. Keinert, C. Haubelt, J. Teich and S. Bhattacharyya.
A Generalized Static Data Flow Clustering Algorithm for MPSoC Scheduling of Multimedia Applications.
In Proc. of the 8th ACM & IEEE international conference on Embedded software (EMSOFT'2008), pp. 189-198, Atlanta, Georgia, USA, October 20-22, 2008.

321 F. Reimann, M. Glaß, M. Lukasiewycz, J. Keinert, C. Haubelt and J. Teich.
Symbolic Voter Placement for Dependability-Aware System Synthesis.
In Proceedings of the 6th International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS), pp. 237-242, Atlanta, GA, USA, October 19-24, 2008.

319 J. Keinert, C. Haubelt and J. Teich.
Automatic Synthesis of Design Alternatives for Fast Stream-Based Out-of-Order Communication.
Proceedings of the 2008 IFIP/IEEE WG 10.5 International Conference on Very Large Scale Integration, (VLSI-SoC 2008), pp. 265-270, Rhodes Island, Greece, October 13-15, 2008.

316 J. Gladigau, C. Haubelt and J. Teich.
Symbolic Quasi-Static Scheduling of Actor-Oriented SystemC Models.
Proceedings of Forum on specification & Design Languages 2008 (FDL08), Digital Object Identifier 10.1109/FDL.2008.4641412, pages 1-6, Stuttgart, Germany, Sep. 23-25, 2008.

315 M. Glaß, M. Lukasiewycz, F. Reimann, C. Haubelt and J. Teich.
Symbolic Reliability Analysis of Self-healing Networked Embedded Systems.
In Proceedings of the 27th International Conference on Computer Safety, Reliability and Security (SAFECOMP 2008), pp. 139-152, Newcastle upon Tyne, UK, September 22-25, 2008.

314 M. Lukasiewycz, M. Glaß and J. Teich.
A Feasibility-preserving Crossover and Mutation Operator for Constrained Combinatorial Problems.
In Proceedings of the 10th International Conference on Parallel Problem Solving from Nature (PPSN 2008), pp. 919-928, Dortmund, Germany, September 13-17, 2008.

312 S. Wildermann and J. Teich.
A Sequential Learning Resource Allocation Network for Image Processing Applications.
Proceedings of the 8th International Conference on Hybrid Intelligent Systems (HIS 2008), pp. 132-137, Barcelona, Spain, September 10-12, 2008.

311 C. Wolinski, K. Kuchcinski, J. Teich and F. Hannig.
Area and Reconfiguration Time Minimization of the Communication Network in Regular 2D Reconfigurable Architectures.
Proceedings of the International Conference on Field Programmable Logic and Applications (FPL), pp. 391-396, Heidelberg, Germany, September 8-10, 2008.

310 C. Claus, W. Stechele, M. Kovatsch, J. Angermeier and J. Teich.
A comparison of embedded reconfigurable video-processing architectures.
Proceedings of 18th International Conference on Field Programmable Logic and Applications (FPL 2008), pp. 587-590, Heidelberg, Germany, September 8-10, 2008.

307 S. Fekete, J. van der Veen, J. Angermeier, D. Koch and J. Teich.
No-Break Dynamic Defragmentation of Reconfigurable Devices.
Proceedings of International Conference on Field-Programmable Logic and Applications (FPL 08), pp. 113-118, Heidelberg, Germany, September 8-10, 2008.

306 D. Koch, C. Beckhoff and J. Teich.
ReCoBus-Builder – a Novel Tool and Technique to Build Statically and Dynamically Reconfigurable Systems for FPGAs.
Proceedings of International Conference on Field-Programmable Logic and Applications (FPL 08), pp. 119-124, Heidelberg, Germany, September 8-10, 2008.

305 R. Schaffer, R. Merker, F. Hannig and J. Teich.
Utilization of all Levels of Parallelism in a Processor Array with Subword Parallelism.
Proceedings of the 11th Euromicro Conference on Digital System Design (DSD), pp. 391-398, Parma, Italy, September 3-5, 2008.

304 C. Wolinski, K. Kuchcinski, J. Teich and F. Hannig.
Communication Network Reconfiguration Overhead Optimization in Programmable Processor Array Architectures.
Proceedings of the 11th Euromicro Conference on Digital System Design (DSD), pp.345-352, Parma, Italy, September 3-5, 2008.

302 M. Glaß, M. Lukasiewycz, R. Wanka, C. Haubelt and J. Teich.
Multi-Objective Routing and Topology Optimization in Networked Embedded Systems.
In Proceedings of the International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation (IC-SAMOS 2008), pp. 74-81, Samos, Greece, July 21-24, 2008.

298 D. Ziener and J. Teich.
Concepts for Autonomous Control Flow Checking for Embedded CPUs.
In Proceedings of the 5th International Conference on Autonomic and Trusted Computing (ATC08), pp. 234-248, Oslo, Norway, June 23-25, 2008.

297 M. Glaß, M. Lukasiewycz, R. Wanka, C. Haubelt and J. Teich.
Multi-Objective Routing and Topology Optimization in Networked Embedded Systems.
In Proceedings of the International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation (IC-SAMOS 2008), Samos, Greece, July 21-24, 2008.

296 D. Ziener and J. Teich.
Concepts for Autonomous Control Flow Checking for Embedded CPUs.
In Proceedings of the 5th International Conference on Autonomic and Trusted Computing (ATC-08), pages 234-248, Oslo, Norway, June 23-25, 2008.

294 M. Lukasiewycz, M. Glaß, C. Haubelt, J. Teich, R. Regler and B. Lang.
Concurrent Topology and Routing Optimization in Automotive Network Integration.
Proceedings of the 2008 ACM/EDAC/IEEE Design Automation Conference (DAC 2008), pages 626-629, Anaheim, CA, USA, June 08-13, 2008.

293 M. Majer, S. Wildermann, J. Angermeier, S. Hanke and J. Teich.
Co-Design Architecture and Implementation for Point-Based Rendering on FPGAs.
Proceedings of the 19th IEEE/IFIP International Symposium on Rapid System Prototyping (RSP 2008), Monterey, CA, USA; June 2-5, 2008.

292 M. Lukasiewycz, M. Glaß, C. Haubelt and J. Teich.
A Feasibility-preserving Local Search Operator for Constrained Discrete Optimization Problems.
Proceedings of the 2008 IEEE Congress on Evolutionary Computation (CEC 2008), Hong Kong, China, June 01-06, 2008.

290 J. Angermeier and J. Teich.
Heuristics for Scheduling Reconfigurable Devices with Consideration of Reconfiguration Overheads.
Proceedings 15th Reconfigurable Architectures Workshop (RAW 2008), Miami, Florida, April 2008.

289 C. Wolinski, K. Kuchcinski, J. Teich and F. Hannig.
Optimization of Routing and Reconfiguration Overhead in Programmable Processor Array Architectures.
Proceedings of the 16th IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM), Palo Alto, CA, USA, April 14-15, 2008.

288 D. Koch, C. Haubelt and J. Teich.
Efficient Reconfigurable On-Chip Buses for FPGAs.
Proceedings 16th Annual IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM 2008), Palo Alto, CA, USA, April 14-15, 2008.

285 F. Hannig, H. Ruckdeschel, H. Dutta and J. Teich.
PARO: Synthesis of Hardware Accelerators for Multi-Dimensional Dataflow-Intensive Applications.
Proceedings of the Fourth International Workshop on Applied Reconfigurable Computing (ARC), Lecture Notes in Computer Science (LNCS), Springer, London, United Kingdom, March 26-28, 2008.

284 J. Angermeier, U. Batzer, M. Majer, J. Teich, C. Claus and W. Stechele.
Reconfigurable HW/SW Architecture of a Reconfigurable HW/SW Architecture of a Real-Time Driver Assistance System.
Proceedings of the Fourth International Workshop on Applied Reconfigurable Computing (ARC), Lecture Notes in Computer Science (LNCS), Springer, London, United Kingdom, March 26-28, 2008.

280 M. Glaß, M. Lukasiewycz, F. Reimann, C. Haubelt and J. Teich.
Symbolic Reliability Analysis and Optimization of ECU Networks.
Proceedings of Design, Automation and Test in Europe (DATE 2008), IEEE Computer Society, Munich, Germany, March 10-14, 2008.

279 M. Streubühr, M. Jäntsch, C. Haubelt, J. Teich and A. Schneider.
Semi-Automatic Generation of mixed Hardware-Software Prototypes from Simulink Models.
11. GI/ITG/GMM-Workshop Methoden zur Modellierung und Verifikation von Schaltungen und Systemen, Freiburg, Germany, pp. 139-148, Freiburg, Germany, March 03-05, 2008.

278 F. Hannig, H. Ruckdeschel and J. Teich.
The PAULA Language for Designing Multi-Dimensional Dataflow-Intensive Applications.
11. GI/ITG/GMM-Workshop Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen, pp. 129-138, Freiburg, Germany, March 03-05, 2008.

277 J. Gladigau, F. Blendinger, C. Haubelt and J. Teich.
Symbolische Modellprüfung Aktor-orientierter High-level SystemC-Modelle mit Intervalldiagrammen.
11. GI/ITG/GMM-Workshop Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen, Freiburg, Germany, pp. 109-118,

March 03-05, 2008.

275 J. Keinert, C. Haubelt and J. Teich.
Synthesis of Multi-Dimensional High-Speed FIFOs for Out-of-Order Communication.
Proceedings of the International Conference on Architecture of Computing Systems (ARCS 2008), pp. 130-143, Dresden, Germany, February 25-28, 2008.

274 R. Brendle, T. Streichert, D. Koch, C. Haubelt and J. Teich.
Dynamic Reconfiguration of FlexRay Schedules for Response Time Reduction in Asynchronous Fault-Tolerant Networks.
Proceedings of the International Conference on Architecture of Computing Systems (ARCS 2008), pp. 117-129, Dresden, Germany, February 25-28, 2008.

273 T. Streichert, M. Glaß, R. Wanka, C. Haubelt and J. Teich.
Topology-Aware Replica Placement in Fault-Tolerant Embedded Networks.
Proceedings of the International Conference on Architecture of Computing Systems (ARCS 2008), pp. 23-37, Dresden, Germany, February 25-28, 2008.

272 S. Wildermann and J. Teich.
Stereo Person Tracking with a Color-Based Particle Filter.
G. Sommer and R. Klette (Eds.): RobVis 2008, LNCS 4931, pp. 327–340, Springer-Verlag Berlin Heidelberg, 2008.

271 F. Hannig, H. Dutta, H. Ruckdeschel and J. Teich.
Quantitative Evaluation of Behavioral Synthesis Approaches for Reconfigurable Devices.
Proceedings of the 2nd HiPEAC Workshop on Reconfigurable Computing, Gothenburg, Sweden, January 27, 2008.

270 M. Lukasiewycz, M. Glaß, C. Haubelt and J. Teich.
Efficient Symbolic Multi–Objective Design Space Exploration.
In Proceedings of the 13th Asia and South Pacific Design Automation Conference (ASP-DAC 2008), pp. 691-696, Seoul, Korea, 2008.

269 D. Koch, C. Beckhoff and J. Teich.
Bitstream Decompression for High Speed FPGA Configuration from Slow Memories.
In Proceedings of the IEEE International Conference on Field-Programmable Technology 2007 (ICFPT'07), pp. 161-168, Kokurakita, Kitayushu, Japan, December 2007.

268 J. Keinert, J. Falk, C. Haubelt and J. Teich.
Actor-Oriented Modeling and Simulation of Sliding Window Image Processing Algorithms.
Proceedings of the 2007 IEEE/ACM/IFIP Workshop of Embedded Systems for Real-Time Multimedia (ESTIMEDIA 2007), pp. 113-118, Salzburg, Austria, Oct. 4-5, 2007.

266 M. Lukasiewycz, M. Glaß, C. Haubelt and J. Teich.
SAT-Decoding in Evolutionary Algorithms for Discrete Constrained Optimization Problems.
In Proceedings of the 2007 IEEE Congress on Evolutionary Computation (CEC 2007), Singapore, Singapore, pp. 935-942, September 25-28, 2007.

263 J. Gladigau, C. Haubelt, B. Niemann and J. Teich.
Mapping Actor-Oriented Models to TLM Architectures.
In Proceedings FDL'07, Forum on Design Languages 2007, Barcelona, Spain, September 18-20, 2007.

257 J. Keinert, C. Haubelt and J. Teich.
Simulative Buffer Analysis of Local Image Processing Algorithms Described by Windowed Synchronous Data Flow.
In Proceedings of the International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation, Acoustics, Speech, and Signal Processing (IC-SAMOS VII), Samos (Greece), July 16-19, 2007.

256 H. Dutta, F. Hannig, A. Kupriyanov, D. Kissler, J. Teich, R. Schaffer, S. Siegel, R. Merker and B. Pottier.
Massively Parallel Processor Architectures: A Co-design Approach.
Proceedings of the 3rd International Workshop on Reconfigurable Communication Centric System-on-Chips (ReCoSoC), pp. 61-68, Montpellier, France, June 18-20, 2007.

255 J. Teich, F. Hannig, H. Ruckdeschel, H. Dutta, D. Kissler and A. Stravet.
A Unified Retargetable Design Methodology for Dedicated and Re-Programmable Multiprocessor Arrays: Case Study and Quantitative Evaluation.
In Proceedings of the International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA), Invited paper, pp. 14-24, Las Vegas, NV, USA, June 25-28, 2007.

254 W. Stechele, O. Bringmann, R. Ernst, A. Herkersdorf, K. Hojenski, P. Janacik, F. Rammig, J. Teich, N. Wehn, J. Zeppenfeld and D. Ziener.
Concepts for Autonomic Integrated Systems.
In Proceedings of edaWorkshop07, Hannover, Germany, June 19-20, 2007.

252 M. Lukasiewycz, M. Glaß, C. Haubelt and J. Teich.
Solving Multiobjective Pseudo-Boolean Problems.
In Proceedings of Tenth International Conference on Theory and Applications of Satisfiability Testing (SAT 2007), pp. 56-69, Lisbon, Portugal, May 28-31, 2007.

251 D. Koch, C. Haubelt, T. Streichert and J. Teich.
Modeling and Synthesis of Hardware-Software Morphing.
In Proceedings of the International Symposium on Circuits and Systems (ISCAS 2007), pp. 2746-2749, New Orleans, LA, USA, May 2007.

249 A. Kupriyanov, D. Kissler, F. Hannig and J. Teich.
Efficient Event-driven Simulation of Parallel Processor Architectures.
In Proceedings of the 10th International Workshop on Software and Compilers for Embedded Systems (SCOPES), pp. 71-80, Nice, France, April 20, 2007.

248 M. Glaß, M. Lukasiewycz, T. Streichert, C. Haubelt and J. Teich.
Reliability-Aware System Synthesis.
In Proceedings of Design, Automation and Test in Europe (DATE 2007), IEEE Computer Society, pp. 409-414, Nice, France, April 16-20, 2007.

246 W. Stechele, O. Bringmann, R. Ernst, A. Herkersdorf, K. Hojenski, P. Janacik, F. Rammig, J. Teich, N. Wehn, J. Zeppenfeld and D. Ziener.
Autonomic MPSoCs for Reliable Systems.
In Proceedings of Zuverlässigkeit und Entwurf (ZuD 2007), pp. 137-138, Munich, Germany, March 26-28, 2007.

245 M. Glaß, M. Lukasiewycz, T. Streichert, C. Haubelt and J. Teich.
Synthese zuverlässiger und flexibler Systeme.
In Proceedings of Zuverlässigkeit und Entwurf (ZuD 2007), pp. 141-148, Munich, Germany, March 26-28, 2007.

244 S. Fekete, J. van der Veen, J. Angermeier, D. Göhringer, M. Majer and J. Teich.
Scheduling and communication-aware mapping of HW-SW modules for dynamically and partially reconfigurable SoC architectures.
In Proceedings of the Dynamically Reconfigurable Systems Workshop (DRS 2007), pages 151-160, Zürich, Switzerland, March 15, 2007.

242 A. Kupriyanov, F. Hannig, D. Kissler, J. Teich, J. Lallet, O. Sentieys and S. Pillement.
Modeling of Interconnection Networks in Massively Parallel Processor Architectures.
In Proceedings of the 20th International Conference on Architecture of Computing Systems (ARCS 2007), Springer LNCS series, Swiss Federal Institute of Technology (ETH), Zurich, Switzerland, pp. 268-282, March 12-15, 2007.

241 M. Lukasiewycz, M. Glaß, C. Haubelt and J. Teich.
Symbolic Archive Representation for a Fast Nondominance Test.
In Proceedings of the Fourth International Conference on Evolutionary Multi-Criterion Optimization (EMO 2007), pp. 111-125, Sendai, Japan, March 5-8, 2007.

240 M. Streubühr, C. Riedel, C. Haubelt and J. Teich.
System Level Modeling and Performance Simulation for Dynamic Reconfigurable Computing Systems in SystemC.
10. Workshop "Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen", pp. 59-68, Erlangen, Germany, March 05-07, 2007.

235 D. Koch, C. Haubelt and J. Teich.
Efficient Hardware Checkpointing -- Concepts, Overhead Analysis, and Implementation.
In Proceedings of the 15th ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA 2007), pp. 188-196, Monterey, CA, USA, February 18-20, 2007.

230 D. Ziener and J. Teich.
FPGA Core Watermarking Based on Power Signature Analysis.
In Proceedings of IEEE International Conference on Field-Programmable Technology (FPT 2006), pp. 205-212, Bangkok, Thailand, December 13-15, 2006.

229 D. Kissler, F. Hannig, A. Kupriyanov and J. Teich.

A Highly Parameterizable Parallel Processor Array Architecture.
In Proceedings of the IEEE International Conference on Field Programmable Technology (FPT 2006), pp. 105-112, Bangkok, Thailand, December 13-15, 2006.

227 D. Kissler, F. Hannig, A. Kupriyanov and J. Teich.
Hardware Cost Analysis for Weakly Programmable Processor Arrays.
In Proceedings of the International Symposium on System-on-Chip (SoC), pp. 179-182, Tampere, Finland, November 14-16, 2006.

226 S. Siegel, R. Merker, F. Hannig and J. Teich.
Communication-conscious Mapping of Regular Nested Loop Programs onto Massively Parallel Processor Arrays.
In Proceedings of the 18th International Conference on Parallel and Distributed Computing and Systems (PDCS), pp. 71-76, Dallas, TX, USA, November 13-15, 2006.

225 J. Teich.
Are Current ESL Tools Meeting the Requirements of Advanced Embedded Systems?.
In Proceedings of the 4th International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS), p. 166, Seoul, Korea, October 22-25, 2006.

223 J. Falk, C. Haubelt and J. Teich.
Efficient Representation and Simulation of Model-Based Designs in SystemC.
In Proceedings FDL'06, Forum on Design Languages 2006, pp. 129 - 134, Darmstadt, Germany, September 19-22, 2006.

222 H. Dutta, F. Hannig and J. Teich.
Hierarchical Partitioning for Piecewise Linear Algorithms.
In Proceedings of the 5th International Symposium on Parallel Computing in Electrical Engineering (PARELEC), pp. 153-159, Bialystok, Poland, September 13-17, 2006.

221 H. Dutta, F. Hannig, J. Teich, B. Heigl and H. Hornegger.
A Design Methodology for Hardware Acceleration of Adaptive Filter Algorithms in Image Processing.
In Proceedings of IEEE 17th International Conference on Application-specific Systems, Architectures and Processors (ASAP), pp. 331-337, Steamboat Springs, CO, USA, September 11-13, 2006.

219 T. Streichert, C. Strengert, C. Haubelt and J. Teich.
Dynamic Task Binding for Hardware/Software Reconfigurable Networks .
In Proceedings of SBCCI 2006, pages 38-43, Ouro Preto, Brasil, August 28th - September 1st, 2006.

218 D. Ziener, S. Aßmus and J. Teich.
Identifying FPGA IP-Cores based on Lookup Table Content Analysis.
In Proceedings of 16th International Conference on Field Programmable Logic and Applications, pp. 481-486, Madrid, Spain, August 28-30, 2006.

217 S. Fekete, J. van der Veen, M. Majer and J. Teich.
Minimizing communication cost for reconfigurable slot modules.
In Proceedings 16th International Conference on Field-Programmable Logic and Applications (FPL 2006), pp. 535-540, Madrid, Spain, August 28-30, 2006.

214 T. Streichert, C. Haubelt and J. Teich.
Multi-Objective Topology Optimization for Networked Embedded Systems.
In Proceedings of the International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation (IC-SAMOS 2006), pp. 93-98, Samos (Greece), July 17-20, 2006.

213 D. Kissler, F. Hannig, A. Kupriyanov and J. Teich.
A Dynamically Reconfigurable Weakly Programmable Processor Array Architecture Template.
In Proceedings of the 2nd International Workshop on Reconfigurable Communication-Centric System-on-Chips (ReCoSoC), pp. 31-37, Montpellier, France, July 3-5, 2006.

212 D. Göhringer, M. Majer and J. Teich.
Bridging the Gap between Relocation and Available Technology: The Erlangen Slot Machine.
In Proceedings of the Dagstuhl Seminar Nº 06141 on Dynamically Reconfigurable Architectures, P. M. Athanas, J. Becker, G. Brebner, J. Teich (Eds.), ISSN 1862 - 4405, Dagstuhl, Germany, April 02-07, 2006.

211 D. Kissler, A. Kupriyanov, F. Hannig, D. Koch and J. Teich.
A Generic Framework for Rapid Prototyping of System-on-Chip Designs.
In Proceedings of the International Conference on Computer Design (CDES), pp. 189-195, Las Vegas, NV, USA, June 2006.

210 D. Koch, M. Körber and J. Teich.
Searching RC5-Keys with Distributed Reconfigurable Computing.
In Proceedings of the International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA 2006), Las Vegas, USA, June 26-29, 2006.

205 J. Keinert, C. Haubelt and J. Teich.
Modeling and Analysis of Windowed Synchronous Algorithms.
In Proceedings of the 31st International Conference on Acoustics, Speech, and Signal Processing (ICASSP2006), Toulouse, France, May 14-19, 2006.

202 M. Majer, A. Ahmadinia, C. Bobda and J. Teich.
A Flexible Reconfiguration Manager for the Erlangen Slot Machine.
In Proceedings of the Dynamically Reconfigurable Systems Workshop (DRS'2006), pp.183-194, Frankfurt/Main, Germany, March 16, 2006.

200 H. Dutta, F. Hannig and J. Teich.
Controller Synthesis for Mapping Partitioned Programs on Array Architectures.
In Proceedings of the 19th International Conference on Architecture of Computing Systems (ARCS), pp. 176-191, Frankfurt/Main, Germany, March 13-16, 2006.

199 D. Koch, T. Streichert, S. Dittrich, C. Strengert, C. Haubelt and J. Teich.
An Operating System Infrastructure for Fault-Tolerant Reconfigurable Networks.
In Proceedings of the 19th International Conference on Architecture of Computing Systems (ARCS 2006), pp. 202-216, Frankfurt/Main, Germany, March 13-16, 2006.

196 M. Streubühr, J. Falk, C. Haubelt, J. Teich, R. Dorsch and T. Schlipf.
Task-Accurate Performance Modeling in SystemC for Real-Time Multi-Processor Architectures.
In Proceedings of Design, Automation and Test in Europe (DATE 2006), pp. 480-481, IEEE Computer Society, Munich, Germany, March 6-10, 2006.

195 T. Schlichter, M. Lukasiewycz, C. Haubelt and J. Teich.
Improving System Level Design Space Exploration by Incorporating SAT-Solvers into Multi-Objective Evolutionary Algorithms.
In Proceedings of *IEEE Computer Society Annual Symposium on VLSI*, pp. 309-314, Karlsruhe, Germany, March 2-3, 2006.

194 A. Kupriyanov, F. Hannig, D. Kissler, J. Teich, R. Schaffer and R. Merker.
An Architecture Description Language for Massively Parallel Processor Architectures.
In Proceedings of the 9th ITG/GMM/GI Workshop, Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen, pp. 11-20, Dresden, Germany, February 20-22, 2006.

193 H. Dutta, F. Hannig and J. Teich.
Mapping of Nested Loop Programs onto Massively Parallel Processor Arrays with Memory and I/O Constraints.
In Friedhelm Meyer auf der Heide and Burkhard Monien, editors, Proceedings of the 6th International Heinz Nixdorf Symposium, New Trends in Parallel & Distributed Computing, volume 181 of HNI-Verlagsschriftenreihe, pp. 97-119, Paderborn, Germany, January 17-18, 2006.

189 A. Ahmadinia, C. Bobda, T. Haller, A. Linarth, M. Majer and J. Teich.
Increasing the Flexibility in FPGA-Based Reconfigurable Platforms: The Erlangen Slot Machine.
In Proc. IEEE 2005 Conference on Field-Programmable Technology (FPT), pages 37-42, Singapore, Singapore, December 11-14, 2005.

186 A. Ahmadinia, C. Bobda, J. Ding, M. Majer and J. Teich.
Modular Video Streaming on a Reconfigurable Platform.
In Proc. IFIP VLSI SOC 2005, pages 103-108, Perth, Australia, October 17-19, 2005.

185 C. Haubelt, M. Jersak, K. Richter, K. Strehl, D. Ziegenbein, R. Ernst, J. Teich and L. Thiele.
SPI-Workbench - Modellierung, Analyse und Optimierung eingebetteter Systeme.
In Proceedings of INFORMATIK 2005 - Informatik LIVE. by Armin B. Cremers, Rainer Manthey, Peter Martini, and Volker Steinhage (Eds.). In Lecture Notes in Informatics. VOL. P-68, No. 2, pp. 693-697, Bonn, Germany, September 19-22, 2005.

184 S. Helwig, C. Haubelt and J. Teich.
Modeling and Analysis of Indirect Communication in Particle Swarm Optimization.

In Proceedings of the 2005 IEEE Congress on Evolutionary Computation, volume 2, pages 1246-1253, Edinburgh, UK, September 02-05, 2005.

183 A. Ahmadinia, C. Bobda, S. Fekete, M. Majer, J. Teich and J. van der Veen.
DyNoC: A Dynamic Infrastructure for Communication in Dynamically Reconfigurable Devices.
In Proceedings of the International Conference on Field-Programmable Logic and Applications (FPL), pp. 153-158, Tampere, Finland, August 24-26, 2005.

182 T. Schlichter, C. Haubelt, F. Hannig and J. Teich.
Using Symbolic Feasibility Tests during Design Space Exploration of Heterogeneous Multi-Processor Systems.
In Proceedings of Application-specific Systems, Architectures and Processors (ASAP). pp. 9-14, Samos, Greece, July 23-25, 2005.

181 H. Ruckdeschel, H. Dutta, F. Hannig and J. Teich.
Automatic FIR Filter Generation for FPGAs.
In Proceedings of the International Workshop on Embedded Computer Systems, Architectures, Modeling, and Simulation (SAMOS), pp. 51-61, Samos, Greece, July 18-20, 2005.

180 F. Hannig and J. Teich.
Output Serialization for FPGA-based and Coarse-grained Processor Arrays.
In Proceedings of the International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA), pp. 78-84, Las Vegas, NV, USA, June 27-30, 2005.

179 F. Hannig, H. Dutta, A. Kupriyanov, J. Teich, R. Schaffer, S. Siegel, R. Merker, R. Keryell, B. Pottier and D. Chillet, D. Ménard, O. Sentieys.
Co-Design of Massively Parallel Embedded Processor Architectures.
In Proceedings of the first ReCoSoC Workshop. Montpellier, France, June 27-29, 2005.

178 A. Ahmadinia, C. Bobda, S. Fekete, F. Hannig, M. Majer, J. Teich and J. van der Veen.
Defragmenting the Module Layout of a Partially Reconfigurable Device.
In Proceedings of the International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA), pp. 92-101, Las Vegas, NV, USA, June 27-30, 2005.

177 T. Schlichter, C. Haubelt and J. Teich.
Improving EA-based Design Space Exploration by Utilizing Symbolic Feasibility Tests.
In Proceedings of *Genetic and Evolutionary Computation Conference* (GECCO), pp. 1945-1952, Washington DC, USA, June 25-29, 2005.

176 A. Ahmadinia, C. Bobda, J. Ding, S. Fekete, M. Majer, J. Teich and J. van der Veen.
A Practical Approach for Circuit Routing on Dynamic Reconfigurable Devices.
In Proceedings of the 16th IEEE International Workshop on Rapid System Prototyping, pp. 84-90, Montreal, Canada, June 8-10, 2005.

174 A. Ahmadinia, C. Bobda, S. Fekete, T. Haller, A. Linarth, M. Majer, J. Teich and J. van der Veen.
The Erlangen Slot Machine: A Highly Flexible FPGA-Based Reconfigurable Platform.
In Proceedings of the 2005 IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM), pp. 319-320, Napa, CA, USA, April 17-20, 2005.

173 T. Dinkel, C. Haubelt, U. Heinkel, J. Knäblein, T. Schlichter, S. Schock and J. Teich.
Comparison of Techniques for the Automatic Verification of ADeVA Specifications.
In Dresdener Arbeitstagung Schaltungs- und Systementwurf (DASS 2005). Dresden, Germany, April 13-14, 2005.

172 T. Dinkel, C. Haubelt, U. Heinkel, T. Schlichter and J. Teich.
Automatische Verification von ADeVA-Spezifikationen.
In Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen. GI/ITG/GMM-Workshop 2005, Munich, Germany, April 06-07, 2005.

171 J. Falk, C. Haubelt and J. Teich.
Representing Models of Computation in SystemC.
In Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen. GI/ITG/GMM-Workshop 2005, Munich, Germany, April 06-07, 2005.

170 A. Ahmadinia, C. Bobda, M. Majer and J. Teich.
Packet Routing in Dynamically Changing Networks on Chip.
In Proceedings of the 12th Reconfigurable Architectures Workshop (RAW 2005), Denver, USA, p. 154b, IEEE Computer Society, April 4-5, 2005.

166 C. Haubelt, J. Gamenik and J. Teich.
Initial Population Construction for Convergence Improvement of MOEAs.
In Evolutionary Multi-Criterion Optimization, Carlos A. Coello Coello, Arturo Hernández Aguirre, and Eckart Zitzler (eds.), Lecture Notes in Computer Science, Vol. 3410, pp. 191-205, Springer, Berlin, Heidelberg, New York, 2005.

165 T. Streichert, C. Haubelt and J. Teich.
Distributed HW/SW-Partitioning for Embedded Reconfigurable Systems.
In Proceedings of DATE 2005, pp. 894-895, Munich, Germany, March 7-11, 2005.

163 T. Streichert, C. Haubelt and J. Teich.
Verteilte HW/SW-Partitionierung für fehlertolerante rekonfigurierbare Netzwerke.
In Proceedings of 17. ITG/GI/GMM Workshop für Testmethoden und Zuverlässigkeit und Fehlertoleranz von Schaltungen und Systemen, pp. 50-54, Innsbruck, Austria, February 27 - March 1, 2005.

162 C. Haubelt, S. Otto, C. Grabbe and J. Teich.
A System-Level Approach to Hardware Reconfigurable Systems.
In Proceedings of Asia and South Pacific Design Automation Conference (ASP-DAC'05), pp. 298-301, Shanghai, China, January 18-21, 2005.

161 T. Streichert, C. Haubelt and J. Teich.
Online Hardware/Software Partitioning in Networked Embedded Systems.
In Proceedings of Asia and South Pacific Design Automation Conference (ASP-DAC'05), pp. 982-985, Shanghai, China, January 18-21, 2005.

Others (Invited Tutorials, Organized Workshops, and Selected Talks)

408 J. Teich.
Invasive Computing - Basic Concepts and Foreseen Benefits.
Artist Network of Excellence on Embedded System Design Summer School Europe 2010, Autrans, France, September 7, 2010, Invited Tutorial.

400 F. Charot, F. Hannig, J. Teich and C. Wolinski.
Proceedings of the 21st IEEE International Conference on Application-specific Systems, Architectures, and Processors (ASAP).
IEEE Computer Society, 2010, ISBN 978-1-4244-6967-3. Editor.

398 J. Teich.
Invasive Computing - A Novel Parallel Computing Paradigm.
Workshop Multiprocessor System-On-Chip (MPSOC): Programmability, Run-Time Support and Hardware Platforms for High Performance Applications, 47th Design Automation Conference (DAC), Anaheim, USA, June 13, 2010. Invited Talk.

390 J. Teich.
Invasives Rechnen.
Sitzung Leitungskreis der Fachgruppe RSS (Rechnergestützter Schaltungs- und Systementwurf), VDE, Frankfurt am Main, April 9, 2010. Invited Talk.

387 J. Teich.
The DFG Priority Program 1148 Reconfigurable Computing - Achievements and Lessons Learned.
DATE Friday Workshop The European Landscape of Reconfigurable Computing: Lessons Learned, new Perspectives and Innovations, Dresden, Germany, March 2010. Invited Talk.

373 V. Schöber, O. Bringmann, A. Herkersdorf, W. Stechele, N. Wehn, M. May, D. Ziener, A. Bouajila, D. Baldin, J. Zeppenfeld, B. Sanders, J. Teich, M. Sebastian, R. Ernst and D. Treytnar.
AIS-Autonomous Integrated Systems.
In Newsletter edacentrum 04 2009, pp. 05-13, edacentrum, Hannover, 2009.

354 J. Teich.
SystemCoDesigner: Automatic Design Space Exploration and Rapid Prototyping from Behavioral Models.
2nd Workshop on MPSoC, ArtistDesign Network of Excellence, St. Goar, Germany, June 29, 2009. Invited Talk.

348 J. Teich and D. Gajski.
The Future of ESL Synthesis.
DATE´09 Friday Workshop W3, Nice, France, 24.3.2009. Workshop Organization.

343 J. Teich and C. Haubelt.
Principles: Analysis, Optimization and Exploration.
DATE´09 Monday Tutorial: System-Level Modeling, Analysis and Synthesis of Embedded Multi-Core Designs, Nice, France, 2009.

300 J. Teich.
Reconfigurability Issues of Future Massively Parallel SoCs.
8th International Forum on Application-Specific Multi-Processor SoC (MPSoC'08), June 23-27, 2008, Aachen, Germany. Invited Talk.

295 J. Teich and F. Schäfer.
ESL Methodologies for Platform-Based Synthesis.
2008 ACM/EDAC/IEEE Design Automation Conference (DAC 2008), Anaheim, USA, June 08-13, 2008. Special Session Organization.

287 J. Teich.
Invasion - A New Parallel Computing and Architecture Paradigm.
Dagstuhl Seminar No. 08141, Organic Computing - Controlled Self-organization, IBFI, March 31- April 4, 2008. Invited Talk.

283 H. Dutta, F. Hannig and J. Teich.
The PARO Design Tool for Automatic Generation of Hardware Accelerators.
Friday Workshop: The New Wave of the High-Level Synthesis, Automation and Test in Europe (DATE), Munich, Germany, March 10-14, 2008.

282 J. Teich, F. Hannig, H. Dutta, D. Kissler and M. Hartl.
Domain-Specific Reconfigurable MPSoC-Systems - Challenges and Trends.
Friday Workshop Reconfigurable Hardware, Design, Automation and Test in Europe (DATE 2008), Munich, Germany, March 14, 2008.

281 D. Kissler, H. Dutta, A. Kupriyanov, F. Hannig and J. Teich.
A High-Speed Dynamic Reconfigurable Multilevel Parallel Architecture.
Hardware and Software Demo at the University Booth at Design, Automation and Test in Europe (DATE), Munich, Germany, March 10-14, 2008.

261 J. Falk, J. Gladigau, C. Haubelt, J. Keinert, T. Schlichter, M. Streubühr and J. Teich.
Substantiating Early Design Decisions by Automatic Design Space Exploration.
16. European SystemC Users Group Meeting, September 18, Barcelona, Spain, 2007. Invited Talk.

243 J. Angermeier, D. Göhringer, M. Majer and J. Teich.
The Erlangen Slot Machine: A flexible FPGA-platform for partially reconfigurable applications at run-time.
20th International Conference on Architecture of Computing Systems (ARCS 2007), Springer LNCS series, Swiss Federal Institute of Technology (ETH) Zurich, Switzerland, March 12-15, 2007. Tutorial.

232 J. Teich.
Evaluation and Optimization of Reliability of Embedded Systems during Design Space Exploration.
Dagstuhl Seminar No. 07101, Quantitative Aspects of Embedded Systems, IBFI, March 5-9, 2007. Invited Presentation.

228 J. Falk, J. Gladigau, C. Haubelt and J. Teich.
SysteMoC - Verification and Refinement of Actor-Based Models of Computation.
ARTIST2 Workshop on MoCC - Models of Computation and Communication, November 16-17, Zurich, Switzerland, 2006. Invited Talk.

220 J. Teich, S. Kaxiras, T. Plaks and K. Flautner.
Topic 18: Embedded Parallel Systems.
Proceedings of12th International Euro-Par Conference, p. 1179, Dresden, Germany, August 28-September 1, 2006. Topic Chair.

216 A. Kupriyanov, F. Hannig, D. Kissler, J. Teich, J. Lallet, O. Sentieys and S. Pillement.
Modeling of Interconnection Networks in Massively Parallel Processor Architectures.
Technical Report 05-2006, University of Erlangen-Nuremberg, Department of CS 12, Hardware-Software-Co-Design, Am Weichselgarten 3, 91058 Erlangen, Germany, August 2006.

203 J. Becker, J. Teich, P. Athanas and G. Brebner.
Dynamically Reconfigurable Architectures.
Proceedings of the Dagstuhl Seminar Nº 06141, ISSN 1862 - 4405, Dagstuhl, Germany, April 02-07, 2006. Workshop Organization.

201 A. Kupriyanov, F. Hannig, D. Kissler, R. Schaffer and J. Teich.
MAML - An Architecture Description Language for Modeling and Simulation of Processor Array Architectures, Part I.
Technical Report 03-2006, University of Erlangen-Nuremberg, Department of CS 12, Hardware-Software-Co-Design, Am Weichselgarten 3, 91058 Erlangen, Germany, March 2006.

198 C. Bobda, M. Platzner and J. Teich.
The Renaissance of FPGA-Based High-Performance Computing.
DATE'06 Friday Workshop, Conference Design Automation and Test in Europe, March 10, 2006, Munich, Germany. Invited Talk.

197 J. Teich, C. Haubelt, D. Koch and T. Streichert.
Concepts for Self-Adaptive Automotive Control Architectures.
DATE'06 Friday Workshop Future Trends in Automotive Electronics and Tool Integration, Conference Design Automation and Test in Europe, March 10, 2006, Munich, Germany. Invited Talk.

192 J. Teich.
Stochastic Timing Analysis of Communicating Tasks with Internal State.
Technical Report 02-2006, University of Erlangen-Nuremberg, Department of CS 12, Hardware-Software-Co-Design, Am Weichselgarten 3, D-91058 Erlangen, Germany,

January 2006.

191 J. Teich.
Timing Analysis of Systems of Communicating Tasks with Internal State.
Technical Report 01-2006, University of Erlangen-Nuremberg, Department of CS 12, Hardware-Software-Co-Design, Am Weichselgarten 3, D-91058 Erlangen, Germany, January 2006.

190 J. Falk, C. Haubelt and J. Teich.
Syntax and execution behavior of SysteMoC.
Technical Report 04-2005, University of Erlangen-Nuremberg, Department of CS 12, Hardware-Software-Co-Design, Am Weichselgarten 3, D-91058 Erlangen, Germany, December 2005.

188 H. Dutta, F. Hannig and J. Teich.
Control Path Generation for Mapping Partitioned Dataflow-dominant Algorithms onto Array Architectures.
Technical Report 03-2005, University of Erlangen-Nuremberg, Department of CS 12, Hardware-Software-Co-Design, Am Weichselgarten 3, 91058 Erlangen, Germany, November 2005.

187 J. Keinert, C. Haubelt and J. Teich.
Windowed Synchronous Data Flow.
Department of Computer Science 12, Hardware-Software-Co-Design, University of Erlangen-Nuremberg, Am Weichselgarten 3, D-91058 Erlangen, Germany Co-Design-Report 02-2005.

169 J. Teich.
Model-Based System-Level Design Using SystemC.
Akademische Tage'05, IBM Forschungslaboratorium, March 18, 2005, Böblingen, Germany. Invited Talk.

168 J. Teich.
The Future of Reconfigurable Computing.
DATE'05 Friday Workshop, Conference Design Automation and Test in Europe, March 11, 2005, Munich, Germany. Workshop Organization.

167 A. Ahmadinia, C. Bobda, T. Haller, A. Linarth, M. Majer and J. Teich.
The Erlangen Slot Machine (ESM): A Flexible Platform for Dynamic Reconfigurable Computing.
Board Demo at the University Booth at Design, Automation and Test in Europe (DATE 2005), Munich, Germany, March 7-11, 2005.

Patente

309 D. Koch, T. Streichert, C. Haubelt and J. Teich.
Logic Chip, Method and Computer Program for Providing a Configuration Information for a Configurable Logic Chip.
Patent PCT/EP2008/007343, filed 8.9.2008.

308 D. Koch, T. Streichert, C. Haubelt and J. Teich.
Logic Chip, Logic System and Method for Designing a Logic Chip.
Patent PCT/EP2008/007342, filed 8.9.2008.

262 D. Koch, T. Streichert, C. Haubelt and J. Teich.
Efficient Reconfigurable On-Chip Buses.
Europäisches Patent EP07017975, Anmeldetag 13.09.2007.

265 D. Ziener and J. Teich.
Watermarking Apparatus, Software Enabling an Implementation of an Electronic Circuit Comprising a Watermark, Method for Detecting a Watermark and Apparatus for Detecting a Watermark.
US-Patent US2007/0220263, Anmeldetag 19.10.2006 aus EP 1835425, veröffentlicht 20.09.2007, Patentklassen (IPC) H04L 9/00.

264 D. Ziener and J. Teich.
Watermarking apparatus, software enabling an implementation of an electronic circuit comprising a watermark, method for detecting a watermark and apparatus for detecting a watermark.
Europäisches Patent EP1835425, Anmeldetag 17.03.2006, veröffentlicht 19.09.2007, Patentklassen (IPC) G06F 17/50; G06F 21/00.