CURRICULUM VITAE of Dr. Per Stenström

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1. Experience

Current Activities:
Professor of Computer Engineering with a Chair in Computer Architecture, Chalmers University of Technology, Göteborg, Sweden since November 1995. My main current activities involve the following:

- **Manager of a Research Program in Computer Architecture.** The research focus is on design principles and design methods for embedded and high-performance computer systems. Research issues span memory system design, architecture support for parallel execution; transactional memory and thread speculation, performance analysis and modeling methodologies, real-time systems, and energy-aware system design tradeoffs. I currently participate in one Integrated EU Project (SARC), a STREP under EU FP7 (VELOX) as well as being a partner in the EU FP7 Network of Excellence HiPEAC. I have also launched the CHAMPP project (Chalmers Adaptive Multi-Processing Project)
- **Teaching.** I annually teach advanced courses on computer architecture (computer architecture and parallel computer systems). I am writing a text book on Computer Architecture with Michel Dubois — my long-term collaborator and dear friend.
- **Professional service to the scientific community.** I service on a regular basis numerous program committees for top conferences in computer architecture and parallel processing and am associate editor of IEEE Computer Architecture Letters since 2001, subject area editor of Journal of Parallel and Distributed Computing since Oct. 1993. I was editor of IEEE Trans. on Computers between 2001 and 2004. I am the founding editor-in-chief of Transactions on HiPEAC which was launched in 2006 and I am an associate editor of IEEE Transactions on Parallel and Distributed Systems.
- **Entrepreneurship.** I am the founder and CTO of Nema Labs AB (founded in 2007) and member of its board of directors. I was the CEO from 2007-2009.

Previous Employments/Appointments:

Adjunct professor at Göteborg University, 2002-2007
Acting Dean of the IT University, 2002-2007

Both these committments had their roots in my active involvement in founding the IT-University in Goteborg. I was recruited to be a member of the Steering Committee to establish the vision and strategic goals of an academic institution that should not only act as an umbrella for academic activities in information technology at Chalmers and Gothenburg University. More importantly, however, it should form an environment that promotes new disciplines that are particularly important for the society. The IT-University went from a project organization to a formal institution in 2002. I contributed to the developments by establishing a Bachelor and Masters program in Software Engineering together with Lars Mathiassen. I also contributed at the managerial level in processes to establish the agenda for the Ph. D. education and the recruitment plans and research funding strategies for this new academic institution.

Visiting Positions in the U.S.A.

I have had the privilege of working with so many wonderful and highly talented individuals in the past in a country that, in my view, is outstanding to leverage on individual assets. The individuals I have been fortunate to collaborate with are listed explicitly below and deserve special mentioning. Besides, my visits in the USA have enriched me at the personal level to a great extent. From a professional standpoint, they boosted my abilities to deliver high quality research and mentorship to young researchers and my understanding of how it can be best transferred to society in efficient ways. I

- **Sun Microsystems** from December 2002 to July 2003. I did my sabbatical in the Advanced System Development Center and investigated concepts for future High-Performance Computer Systems. My manager there was vice-president Dr. Rick Lytel.
- **University of Southern California, Department of EE-Systems** from July 1993 to September 1993. Worked with Professor Michel Dubois on the specification of the architecture of an experimental shared-memory multiprocessor system. Michel and I have continously worked together since 1990.
- **Stanford University, Computer Systems Laboratory** from June 1991 to December 1991. Worked with Professor Anoop Gupta on performance evaluation and architectural innovation of scalable shared-memory multiprocessor architectures. We developed the Flat-COMA proposal during that time.
- **Carnegie-Mellon University, Department of Computer Science** from September 1987 to May 1988. Worked with Professor Zary Segall on implementation and evaluation of shared-memory models on distributed system architectures. We evaluated one of the first shared-memory model implementations on a distributed system.

In the really early phases of my career, I did the following

Associate Professor of Computer Engineering, Lund University, Sweden, from November 1993 until November 1995 (before that on the faculty since July 1988 and a Ph. D. student since February 1984).

- Taught graduate and undergraduate courses in Computer Architecture, Switching Theory, and Hardware Design. I developed a textbook on basic computer organization and assembly language programming that was printed by Prentice Halls,
- Led a research group since 1990 in Parallel Computer Architecture. I supervised three Ph. D. students that successfully earned their degrees until my move to Chalmers. My group was very successful; we got five ISCA papers accepted during the five years this group existed before I left for a full professorship at Chalmers.

- Was Director of Studies at the department since July 1988.
- Was member of the Board of the Graduate School of Electrical and Computer Engineering at Lund University since November 1993.
- Was acting full professor from January 1995 until June 1995

Advisory Roles, Consultancy, and Commisions of Trust in academeia and industry

- **Scientific advice.** I was a scientific advisor of the Swedish Institute of Computer Science between 1995 and 1998.
- **Chair of the council for the faculty at the School of Electrical and Computer Engineering.** Between July 1998 until I became a vice-dean in April 1999.
- **Vice-Dean of the School of Electrical and Computer Engineering.** 1999-2001.
- **Vice-Dean of the School of Computer Science and Engineering at Chalmers.** 2001-2003.
- **Member of the board of Blekinge Institute of Technology.** 2001-2004.
- **Program Coordinator for three bigger efforts:**

  PAMP (1998-2003) (Performance-demanding Applications on Multi-Processors) is a project funded by The Foundation for Strategic Resaearch which involves research groups at five research institutions and five companies across the country. The focus is on software and hardware design methods for using multiprocessors in industrial applications. The program ran for five years (from 1998-2003) with an annual budget of 5 MSEK and is sponsored by the Swedish Foundation for Strategic Research (SSF).The output of the number was truly amazing with some ten PhDs.

  FLEXSOC (2003-2007), The objective of this project was to build a heterogeneous SOC platforms of a wide variety of core functionalities and make it significantly more programmable and energy-efficient. Our approach to make it more programmable was to define an architecture framework in which accelerators could be added with a low performance cost and engineering cost as possible.

  We managed to show that are unifying approach - called FlexCore - to host application-specific accelerators with general-purpose cores is feasible and it can yield lower energy consumption. In an evaluation of the project, one comment was that we have achieved a lot despite the limited funds.

  CHAMMP (2010-2014). This project got funding inn November 2009 from the Swedish Research Council and aims at resources on a multicore chip are best expended to provide high performance across a large set of applications with acceptable energy loss. Our approach is to add adaptivity to processor cores as well as the memory system.

- **Chair of Research Evaluation Panel in Computer Science.** I was the chair of the group to evaluate research proposals sent to the Computer Science area in the Swedish Research Council between 2001 and 2005. My main role was to make sure that all applications are fairly evaluated by putting together a trustful panel and soliciting a large number of external reviewers. It was a very good experience to learn how to deal with many promising proposals and really make the best to bet on the right horses in an as solid way as possible.

- **Board of directors.** Virtutech AB (1998 - 2002), I owned the technical perspective here and helped the rest of my board colleagues to understand what where the most strategic directions to take into the plan for company growth. Virtutech is today a solid company located in the US. This mission not only introduced me to the world of start-tups but also made it clear that I should try the same one day.
- **Technical advisor.** Imsys AB (2001-2003) I helped this Swedish processor company to position themselves among other processors.
- **Consultancy.** Sun Microsystems Inc. (2003-2006) I worked with Sun in capacity as an expert and was called in to take part in various design reviews. I also contributed with a lot of IPR and filed about eight patents.
- **Member of the Board** of the IT University of Goteborg. 2006 - 2009.
- **Member of research priority panel for the Swedish Strategic Research Foundation** (2006-2007) in the area of software. I pushed especially our need of a strategy towards multicore computers.

2. Academic degrees

Docent degree in Electrical and Computer Engineering at Lund University

November 1993.

Ph. D. degree in Computer Engineering

Thesis title: *Aspects of Memory Systems for MIMD Multiprocessors with a Shared-Memory Model*, Department of Computer Engineering, Lund University, May 1990. Thesis advisor: Prof. Lars Philipson

Master of Science in Electrical Engineering:

Thesis title: *Digital in- och uppspelning av deltamodulerat tal* (in Swedish), Department of Computer Engineering, Lund University, October 1981. Thesis advisor: Prof. Lars Philipson

3. Research Focus

My whole research production has centered on the general question how to design general-purpose computer systems to deliver a high performance within the constraints of the technology and given current application and technology trends. In focusing on this general question, it has been important to me to take a holistic system view in addressing how applications, system software, and compiler technology interact with the hardware platform and how performance can be improved by design tradeoffs across the hardware/software boundary. My research has focused on improving multiprocessor technology mainly.

The key contributions I have made to the field of computer architecture concerns:

- *Shared-memory multiprocessor architecture*; specifically design of high-performance memory systems. I have made considerable contributions to the design of multiprocessor systems, especially how to make them scale to a large number of processors. I have been a key contributor to the general understanding of how to use caches in such systems to overcome the memory system bottleneck by a range of innovations regarding cache coherence maintenance, latency tolerance techniques, and hardware/software tradeoffs in supporting memory consistency models. This work has been very influential.
- *Compiler optimization techniques;* specifically to remove performance overhead associated with cache coherence maintenance. My early work on using dataflow analysis techniques to reduce latency and bandwidth associated with loads and stores to shared data has been quite pioneering. This work has yielded lots of citations.

- *Performance evaluation methodologies*; specifically simulation techniques based on direct execution and analytical models. I have contributed with improved methodologies for full system simulation by leading the developments of the CacheMire test bench and participated in the developments of Simics, a full system simulation platform. I've also recently developed an analysis method that can make accurate estimates of the worst-case execution time of programs on high-performance processors taking caching and multiple-issue pipelining techniques into consideration. This work has been very influential.
- *Thread-level speculative execution.* Over the last several years, I've taken an interest in simplifying the task of extracting coarse-grained (or thread-level) parallelism out of sequential programs recognizing the possible trend of migrating multiprocessor support to the chip level. I've run several projects in which we consider hardware/software tradeoffs in the implementation of efficient speculation mechanisms and in how to extract module-level parallelism, i.e., parallelism across procedures, functions, and methods. This project has led to great insights on how to support this paradigm both at the hardware as well as the software level. It has been influential.
- A natural continuation of this work is on transactional memory which builds on cache coherence work I did in the past and my more recent focus on identifying useful support at the architectural level to ease parallel programming. My group has explored a wide range of hardware protocols for implementation of transactional memory with the goal of making them efficient and yet reasonably simple to implement to accelerate deployment in industry. This is ongoing work.
- *Design tradeoffs for high performance under power consumption constraints.* Another recent interest concerns how to do design tradeoffs to maximize the performance under energy dissipation constraints. My goal is to understand what affects architectural tradeoffs regarding high-performance memory system design and methodologies to aid designers in making such tradeoffs. A project with Ericsson Mobile Communication in which we especially consider architectural techniques to fuel the development of powerful handheld computers/phones. This project yielded many interesting results. We came up with energy-efficient cache coherence solutions and helped defined the key concept for snoop filtering which is widely used in machines today. We continued to look at techniques to improve utilization of memory resources. Our work on memory compression and multi-level memory hierarchies has triggered a lot of research in our footsteps.

4. Teaching

My teaching experience ranges from developments of individual courses to specializations (suites of courses) in Computer Engineering. Apart from course developments, I have a strong interest in developing new pedagogical approaches to teach topics in complex engineering systems.

- I have taught courses on Digital Design, Computer Organization, Computer Architecture, and Parallel Computer Architecture over the past two decades.
- I've also been involved in curriculum design. In 1997 I led the development of an advanced program within the computer science and engineering curriculum in computer systems engineering. The program is intended to provide an in-depth coverage of technologies and design methods for application-specific computer systems.
- I'm author of two textbooks on Computer Organization and Assembly Language Programming (see Section 5.1) and another one is scheduled for release in 2010.

- I have developed advanced laboratories for courses in computer architecture; the one on instruction pipelining (see conference paper 14 in Section 5.3) is a good example. It has been used in classes at Lund University and Chalmers University of Technology for 15 years which gives a token for its fundamental nature!
- I have offered several tutorials and graduate courses at summer schools (CNRS, France, 1994; ARTES, Stockholm, Sweden, 1998), institutions (UPC Barcelona, 1998, 2002), companies (Ericsson 1998), and conferences (EuroPar95 and EuroPar97), as well as being an invited speaker on educational issues (the IEEE CAEWS workshop) .
- I gave a two-week intensive Ph. D. course (24 hours) on shared-memory multiprocessors at UPC in Barcelona in April 2002.
- I gave a course on chip multiprocessors in Italy (http://escher.elis.ugent.be/hipeac/summerschool/) in conjunction with the 1st HiPEAC summer school, July 2005.
- I will give a course on "Methods to Transfer Research To Business" with Andrzej Brud of Chalmers Innovation at the 5th HiPEAC summer school, July 2010.

5. Publications

5.1 Textbooks

1. L. Ohlsson and P. Stenström: "Computer Organization and Assembly Language Programming," Studentlitteratur and Chartwell-Bratt, ISBN 91-44-26461-5, January 1987.
2. P. Stenström: ''68000 Microcomputer Organization and Programming," Prentice-Hall, ISBN 0-13-584855-5, September 1992.
3. Michel Dubois and Per Stenström . *Parallel Computer Organization and Design.* with Cambridge Press. Forthcoming 2010.

5.2 Journal Papers

4. P. Stenström: "Reducing Contention in Shared-Memory Multiprocessors," in *IEEE Computer*, Vol 21, No 11, pp. 26-37, November 1988.
5. P. Stenström: "A Survey of Cache Coherence Schemes for Multiprocessors," in *IEEE Computer*, Vol 23, No 6, pp. 12-24, June 1990.
6. H. Grahn, P. Stenström, and M. Dubois: "Implementation and Evaluation of Update-Based Cache Protocols Under Relaxed Memory Consistency Models," in *Future Generation Computer Systems*, Vol. 11, No. 3, pp. 247-271, June 1995.
7. F. Dahlgren and P. Stenström: "Using Write Caches to Improve Performance of Cache Coherence Protocols in Shared-Memory Multiprocessors," in *Journal of Parallel and Distributed Computing*, Vol 26. No 2, pp. 193-210, April 1995.
8. F. Dahlgren, M. Dubois, and P. Stenström: "Sequential Hardware Prefetching in Shared-Memory Multiprocessors," in *IEEE Trans. on Parallel and Distributed Systems,* Vol. 6 No 7, pp. 733-746, July 1995.
9. M. Dubois, J. Skeppstedt, and P. Stenström: "Essential Misses and Memory Traffic in Coherence Protocols," in *Journal of Parallel and Distributed Computing*, Vol. 29, No 2, pp. 108-125, October 1995.
10. F. Dahlgren and P. Stenström "Evaluation of Stride and Sequential Hardware-based Prefetching in Shared-Memory Multiprocessors," in *IEEE Trans. on Parallel and Distributed Systems*, Vol. 7, No. 4, pp. 385-398, April 1996.

11. M. Brorsson and P. Stenström: “Characterising and Modelling Shared-Memory Accesses in Multiprocessor Programs,” in *Parallel Computing*, No 22, pp. 869-893, 1996.

12. P. Stenström, M. Balldin, and J. Skeppstedt: “The Design of a Non-Blocking Load Processor Architecture,” in *Microprocessors and Microsystems, No 20, pp. 111-123,* 1996.

13. H. Grahn and P. Stenström: “Evaluation of an Adaptive Update-Based Cache Protocol,” in *Journal of Parallel and Distributed Computing,* 39(2):168-180, December 1996.

14. J. Skeppstedt and P. Stenstrom. Using Dataflow Analysis Techniques to Reduce Ownership Overhead in Cache Coherence Protocols. In *ACM Transactions on Computer Systems,* Vol. 18, No 6., pp. 659-682, November 1996

15. P. Stenström, M. Brorsson, F. Dahlgren, H. Grahn, and M. Dubois: “Boosting Performance of Shared-Memory Multiprocessors,” in *IEEE Computer,* pp. 63-70, July 1997.

16. M. Karlsson and P. Stenström: “Effectiveness of Dynamic Prefetching in Multiple-Writer Distributed Virtual Shared Memory Systems,” in *Journal of Parallel and Distributed Computing*, Vol. 43, No. 2, pp. 79-93, 1997.

17. F. Dahlgren, M. Björkman and P. Stenström: “Reducing the Read Miss Penalty for Flat COMA Protocols, in *the Computer Journal*, Vol. 40, No. 4, pp. 208-219, 1997.

18. P Stenström, Erik Hagersten, David Lilja, Margaret Martonosi, and Madan Venugopal: “Trends in Shared-Memory Multiprocessing,” in *IEEE Computer*, Vol. 30, No. 12, pp. 44-50, December 1997.

19. F. Dahlgren, J. Skeppstedt, and P. Stenström: “An Evaluation of Hardware-Based and Compiler-Controlled Snooping Cache Protocol Extensions,” in *Journal of Future Generation Computer Systems,* No. 13, pp. 469-487, 1998.

20. F. Dahlgren, M. Dubois, and P. Stenström: “Performance Evaluation and Cost Analysis of Cache Protocol Extensions for Shared-Memory Multiprocessors,” in *IEEE Transactions on Computers*, Vol. 47, No 10, pp. 1041-1055, Oct. 1998.

21. J. Skeppstedt, F. Dahlgren, and P. Stenström: “Evaluation of Compiler-Controlled Updating to Reduce Coherence-Miss Penalties in Shared-Memory Multiprocessors,” in *Journal of Parallel and Distributed Computing,* Vol. 56, No 2, pp. 122-153, 1999.

22. T. Lundqvist and P. Stenström: “An Integrated Path and Timing Analysis Method Based on Cycle-Level Symbolic Execution,” In *Journal of Real-Time Systems,* 17 (2/3):183-207, November 1999.

23. H. Grahn and P. Stenström: “Comparative Evaluation of Latency-Tolerating and Reducing Techniques for Hardware-Only and Software-Only Directory Protocols”, *Journal of Parallel and Distributed Computing,* Vol. 60, No. 7, pp. 807-834, July 2000.

24. J. Jalminger and P. Stenström “Improving Energy-Efficiency in Off-Chip Caches using Selective Prefetching”, In *Journal of Microprocessors and Microsystems,* No 26, pp. 107-121, 2002.

25. P. Rundberg and P. Stenström: An All-Software Thread-Level Data Dependence Speculation System for Multiprocessors,” *Journal of Instruction-Level Parallelism,* Vol 3. Oct 2002.

26. Håkan Grahn and Per Stenström. A Comparative Evaluation of Hardware-Only and Software-Only Directory Protocols in Shared-Memory Multiprocessors, *Journal of Systems Architecture,* Vol 50 (2004) pages 537-561.

27. Jonas Jalminger and Per Stenstrom: A Cache Block Reuse Prediction Scheme. *Journal of Microprocessors and Microsystems.* Vol 28 (2004), pages 373-385.

28. K. De Bosschere, G. Gaydadjiev, X. Martorell, N. Navarro, M. O'Boyle, D. Pnevmatikatos, A. Ramirez, P. Sainrat, A. Seznec, P. Stenstrom, and O. Temam. High-Performance Embedded Architecture and Compilation Roadmap. In *Transactions on High-Performance Embedded Architectures and Compilers.* Vol 1, No 3. Dec. 2006.

29. J. Chen, M. Dubois, and P. Stenstrom: Integrating Complete-system and User-level Performance/Power Simulators: the SimWattch Approach. In *IEEE Micro* Magazine, July-August, 2007.

30. J. Hollmann, A. Ardo, Per Stenstrom: The Effectiveness of Caching in a Distributed Digital Library. In *Journal of System Architecture,* pages 53(7) 403-416, 2007.

31. Mafijul Islam, Magnus Själander, and Per Stenstrom. Early Detection and Bypassing of Trivial Operations to Reduce Energy. Accepted for publication in *Journal of Microprocessors and Microsystems*. October 2007.

32. Martin Thuresson, Magnus Själander, Magnus Björk, Lars Svensson, Per Larsson-Edefors, Per Stenstrom. FlexSoC: Utilizing Exposed Datapath Control for Efficient Computing. Accepted for publication in *Journal of VLSI,* December 2007.

33. P. Stenstrom. The Paradigm Shift to Multi-Cores: Opportunities and Challenges. In Journal of *Applied and Computational Mathematics.* Vol 6, No 2, pages 253-257, 2007.

34. Reinhard Wilhelm, Jakob Engblom, Andreas Ermedahl, Niklas Holsti, Stephan Thesing, David B. Whalley, Guillem Bernat, Christian Ferdinand, Reinhold Heckmann, Tulika Mitra, Frank Mueller, Isabelle Puaut, Peter P. Puschner, Jan Staschulat, Per Stenstrom. The Determination of Worst-Case Execution Times — Overview of Methods and Survey of Tools. *ACM Trans. Embedded Comput. Syst*. 7(3): (2008)

35. F. Warg and P. Stenstrom. Dual-Thread Speculation: A Simple Approach to Uncover Thread-Level Parallelism on a Simultaneous Multithreaded Processor. *International Journal of Parallel Programming* 36(2): 166-183 (2008)

36. M. Thuresson, L. Spracklen, P. Stenstrom. Memory Link Compression Schemes: A Value Locality Perspective. *IEEE Transactions on Computers,* Jan 2008.

37. M. M. Waliullah and P. Stenstrom. Schemes for Avoiding Starvation in Transactional Memory Protocols. in *Journal of Concurrency and Computation: Practice and Experience*. Vol 21, No 7, pp. 859-873, 2009.

38. Jaeheon Jeong, Per Stenstrom, and Michel Dubois. Simple Penalty-Sensitive Cache Replacement Policies. *Journal of ILP.* Vol 10, July 2008.

39. J. Chen, Jianwei, M. Dubois, and P. Stenstrom, Per: SimWattch and Learn. *IEEE Potentials*, 28 (1) pp. 17-23, 2009.

5.3 Conference Papers (refereed)

40. P. Stenström and L. Philipson: "A layered emulator for design evaluation of MIMD multiprocessors with shared memory," in *Proc. of PARLE (Parallel Architectures and Languages Europe)*, Lecture Notes in Computer Science, No 258, Springer-Verlag, pp. 329-344, June 1987.

41. P. Stenström: "VLSI Support for a Cactus Stack Oriented Memory Organization," in *Proc. of the 21st Hawaii International Conference on System Sciences*, pp. 211-220, January 1988.

42. P. Stenström, D. Vrsalovic, and Z. Segall: "Shared Data Structures in a Distributed System — Performance Evaluation and Practical Considerations," in *Proc. of IFIP TC 7/WG 7.3, International Seminar on Performance of Distributed and Parallel Systems*, pp. 15-30, December 1988.

43. P. Stenström: “A Cache Consistency Protocol for Multiprocessors with Multistage Networks,” in *Proc. of 16th Annual International Symposium on Computer Architecture*, pp. 407-415, May 1989.

44. P. Stenström, F. Dahlgren, and L. Lundberg: “A Lockup-free Multiprocessor Cache Design,” in *Proc. of International Conference on Parallel Processing*, Vol 1, pp 246-250, August 1991.

45. F. Dahlgren and P. Stenström: “On Reconfigurable On-chip Data Caches,” in *Proc. of 24th ACM/IEEE International Symposium on Microarchitectur*e, pp. 189-198, November 1991.

46. F. Dahlgren and P. Stenström: “Reducing Write Latencies for Shared Data in a Multiprocessor with a Multistage Network,” in *Proc. of 25th Hawaii International Conference on System Sciences*, pp. 449-456, January 1992.

47. P. Stenström: “A Latency-Hiding Scheme for Multiprocessors with Buffered Multistage Networks,” in *Proc. of International Parallel Processing Symposium*, pp. 39-42, March 1992.

48. P. Stenström, T. Joe, and A. Gupta: “Comparative Performance Evaluation of Cache-Coherent NUMA and COMA Architectures,” in *Proc. of 19th Annual International Symposium on Computer Architecture*, pp. 80-91, May 1992.

49. H. Nilsson and P. Stenström: “The Scalable Tree Protocol — A Cache Coherence Approach for Large-Scale Multiprocessors,” in *Proc. of Fourth IEEE Symposium on Parallel and Distributed Processing*, pp. 498-507, December 1992.

50. M. Brorsson and P. Stenström: “Visualising Sharing Behaviour and its Relation to Shared Memory Management,” in *Proc. of 1992 International Conference on Parallel and Distributed Systems*, pp. 528-536, December 1992.

51. H. Nilsson and P. Stenström: “Performance Evaluation of Link-Based Cache Coherence Schemes,” in *Proc. of 26th Hawaii International. Conference on System Sciences*, pp. 486-495, January 1993.

52. P. Stenström, H. Nilsson, and J. Skeppstedt: “Using Graphics and Animation to Visualize Instruction Pipelining and its Hazards,” in *Proc. of ICSEE'93*, pp. 130-135 January 1993.

53. M. Brorsson, F. Dahlgren, H. Nilsson, and P. Stenström: “The CacheMire Test Bench—A Flexible and Effective Approach for Simulation of Multiprocessors,” in *Proc. of 26th IEEE Annual Simulation Symposium*, pp. 41-49, March 1993.

54. P. Stenström, M. Brorsson, and L. Sandberg: “An Adaptive Cache Coherence Protocol Optimized for Migratory Sharing,” in *Proc. of 20th ACM/IEEE Annual International Symposium on Computer Architecture*, pp. 109-118, May 1993.

55. M. Dubois, J. Skeppstedt, L. Ricciulli, K. Ramamurthy, and P. Stenström: “The Detection and Elimination of Useless Misses in Multiprocessors,” in *Proc. of 20th ACM/IEEE Annual International Symposium on Computer Architecture*, pp. 88-97, May 1993.

56. F. Dahlgren, M. Dubois, and P. Stenström: “Fixed and Adaptive Sequential Prefetching for Shared-Memory Multiprocessors,” in *Proc. of 1993 International Conference on Parallel Processin*g, pp. 56-63, August 1993.

57. F. Dahlgren, M. Dubois, and P. Stenström: “Combined Performance Gains of Simple Cache Protocol Extensions, in *Proc. of 21st ACM/IEEE Annual International Symposium on Computer Architecture*, pp. 187-197, April 1994.

58. H. Nilsson and P. Stenström: “An Adaptive Update-Based Cache Coherence Protocol for Reduction of Miss Rate and Traffic,” *in Proc. of PARLE (Parallel Architectures and Languages Europe)*, pp. 363-374, June 1994. Best Paper Award at the conference.

59. F. Pong, P. Stenström, and M. Dubois: “An Integrated Methodology for Verification of Correctness of Cache Coherence Protocols” in *Proc. of 1994 International Conference on Parallel Processing*, pp. 158-165, August 1994.

60. F. Dahlgren and P. Stenström: “Reducing the Write Traffic for a Hybrid Cache Protocol,” in *Proc. of 1994 International Conference on Parallel Processing*, pp. 166-173, August 1994.

61. J. Skeppstedt and P. Stenström: “Simple Compiler Algorithms to Reduce Ownership Overhead in Cache Coherence Protocols,” in *Proc. of 6th ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS VI*), pp. 286-296, October 1994.

62. M. Brorsson and P. Stenström: “Modelling Accesses to Stationary Data in Shared Memory Multiprocessors,” in *Proc. of the 7th International Conference on Parallel and Distributed Computing (PDCS'94)*, pp. 802-807, October 1994.

63. M. Brorsson and P. Stenström: “Modelling Accesses to Migratory and Producer-Consumer Characterised Data in a Shared Memory Multiprocessor,” in *Proc. of Sixth IEEE Symposium on Parallel and Distributed Processing*, pp. 612-619, October 1994.

64. M. Björkman, F. Dahlgren, and P. Stenström: “Using Hints to Reduce Read Miss Penalties for Flat COMA Protocols, in *Proc. of 28th Hawaii International Conference on System Sciences*, pp. 242-251, January 1995.

65. F. Dahlgren and P. Stenström “Effectiveness of Stride and Sequential Hardware-based Prefetching in Shared-Memory Multiprocessors, in *Proc. of First International Conference on High Performance Computer Architecture (HPCA-1)*, pp. 68-77, January 1995.

66. H. Grahn and P. Stenström: “Efficient Strategies for Software-Only Directory Protocols in Shared-Memory Multiprocessors,” in *Proc. of 22nd ACM/IEEE Annual International Symposium on Computer Architecture*, pp. 38-47, June 1995.

67. J. Skeppstedt and P. Stenström: “A Compiler Algorithm that Reduces Read Latency in Ownership-Based Cache Coherence Protocols,” in *Proc. of Parallel Architectures and Compilation Techniques*, pp. 69-78, July 1995.

68. F. Dahlgren, J. Skeppstedt, and P. Stenström: “Effectiveness of Hardware-Based and Compiler-Controlled Snooping Protocol Extensions,” in *Proc. of the International Conference on High Performance Computing, pages 87-92*, December 1995.

69. M. Karlsson and P. Stenström: “Performance Evaluation of a Cluster-Based Multiprocessor Built from ATM-Switches and Bus-Based Multiprocessor Servers,” in *Proc. of Second International Conference on High Performance Conputer Architecture*, pages 4-13, Jan. 1996.

70. H. Grahn and P. Stenström: “Relative Performance of Software-Only and Hardware-Only Directory Protocols Under Latency Tolerating and Reducing Techniques,” in *Proceedings of the 11th International Parallel Processing Symposium*, pages 500-506, April 1997.

71. P. Stenström and J. Skeppstedt: “A Performance Tuning Approach for Shared-Memory Multiprocessors” in *Proceedings of EUROPAR’97*, pp. 72-84, August 1997.

72. J. Nilsson, F. Dahlgren, M. Karlsson, P. Magnusson, P. Stenström: “Computer System Evaluation with Commercial Workloads” in *Proc. of IASTED Conference on Modeling and Simulation*. pp. 293-297, May 1998.

73. P Magnusson, F Dahlgren, H. Grahn, M. Karlsson, F. Larsson, A. Moestedt, J. Nilsson, P Stenström, and B. Werner: “SimICS/Sun4m: A Virtual Workstation. In *Proc. of USENIX98*,pp. 119-130, June 1998.

74. T. Lundqvist and P. Stenström: “Timing Anomalies in Dynamically Scheduled Processors,” in *Proc. of 1999 IEEE Real-Time System Symposium (RTSS’99)*, pp. 12-21 Dec. 1999.

75. T. Lundqvist and P. Stenström. “A Method to Improve the Estimated Worst-Case Performance of Data Caching”. in *Proc. of 6th International Conference on Real-Time Computing Systems and Applications (RTCSA'99)*, pp. 255-262, Dec 1999.

76. M. Karlsson, F. Dahlgren, and P. Stenström: “A Prefetching Technique for Irregular Accesses to Linked Data Structures,” *6th IEEE Int. Symp. on High-Performance Computer Architecture (HPCA-6)*, pp. 206-217, 2000.

77. M. Karlsson, F. Dahlgren, and P. Stenström: “An Analytical Model for Working-Set Sizes in Decision Support Systems,” In *Proc. of* ACM *SIGMETRICS*,pp. 275-285, 2000.

78. A. Saulsbury, F. Dahlgren, and P. Stenström: “Recency-Based TLB Preloading” in *27th ACM/IEEE Int. Symp. on Computer Architecture (ISCA-27)*, pp. 117-127, 2000.

79. U. Assarsson and P. Stenström: Evaluation of Load-Distribution Strategies for Hierarchical View Frustum Culling and Collision Detection. in *EuroPar 2001*, pages 663-673, Aug 2001.

80. F. Warg and P. Stenström: Limits on Speculative Module-Level Parallelism in Imperative and Object-Oriented Programs on CMP Platforms. In *Proc. of Int. Conf. on Parallel Architectures and Compiler Techniques (PACT’2001)*, pages 221-230, Sept. 2001.

81. M. Kämpe, P. Stenström, M. Dubois: The FAB Predictor: Using Fourier Analysis to Predict the Outcome of a Conditional Branch. In *Proc. of 8th IEEE Int. Symp. on High-Performance Computer Architecture (HPCA-8)*, February 2002.

82. M. Ekman, F. Dahlgren, and P. Stenström: “TLB and Snoop Energy-Reduction using Virtual Caches for Low-Power Chip-Multiprocessors”. In *Proc. of ACM ISLPED-2002*.

83. Jianwei Chen, Michel Dubois, and P. Stenstrom: SimWattch: An Approach to Integrate Complete-System with User-Level Performance/Power Simulators. In Proc. of *IEEE ISPASS-2003*, March 2003.

84. J. Nilsson, A. Landin, P. Stenström: Coherence Predictor Cache: A Resource Efficient Coherence Message Prediction Infrastructure. In *6th IEEE International Symposium on Parallel and Distributed Processing Symposium*, April 2003.

85. P. Rundberg and P. Stenström: Speculative Lock Reordering: Optimistic Out-of-Order Execution of Critical Sections. In *6th IEEE International Symposium on Parallel and Distributed Processing Symposium*, April 2003.

86. F. Warg and P. Stenström: Improving Speculative Thread-Level Parallelism through Module Run-Length Prediction. In *6th IEEE International Symposium on Parallel and Distributed Processing Symposium*, April 2003.

87. J. Hollmann, A. Ardö, P. Stenström: Evaluation of Document Prefetching in a Distributed Digital Library. March 2003. In Proc. of *7th European Conference and Research on Advanced Technology for Digital Libraries (ECDL’2003)*.

88. J. Jalminger and P. Stenström: A Novel Approach to Cache Block Reuse Prediction. In *Proc. of International Conference on Parallel Processing*, Oct. 2003.

89. M. Ekman and P. Stenstrom: Performance and Power Impact of Issue-width in Chip-Multiprocessor Cores. *In Proc. of International Conference on Parallel Processing*, Oct. 2003.

90. John Hughes, Kjell Jeppsson, Per Larsson-Edefors, Mary Sheeran, Per Stenstrom, Lars “J” Svensson, *FlexSoC: Combining Flexibility and Efficiency in SoC Designs*. in IEEE Norchip 2003 Conference. November 2003.

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92. Magnus Ekman and Per Stenstrom. Enhancing Simulation Speed using Matched-Pair Comparison. In *Proc. of 2005 IEEE ISPASS*. April 2005.

93. Magnus Ekman and Per Stenstrom. A Cost-Effective Memory Organization for Future Servers. In *Proc. of 2005 IEEE Int. Parallel and Distributed Processing Symposium.*

94. Fredrik Warg and Per Stenstrom: Reducing Misspeculation Overhead for Module-Level Speculative Execution. In *ACM Computing Frontiers.* May 2005.

95. Martin Thuresson and Per Stenstrom. Evaluation of Extended Dictionary-Based Static Code Compression Techniques. In *ACM Computing Frontiers.* May 2005.

96. Magnus Ekman and Per Stenstrom: A Robust Memory Compression Scheme. *In the 32nd IEEE/ACM Ann. Int. Symposium on Computer Architecture.* Madison, June, 2005.

97. E. Vallejo, M. Galluzi, A. Cristal, F. Vallejo, R Beivide, P. Stenstrom, J. Smith, M. Valero. Implementing Kilo-Instruction Multiprocessors. In *Proc. of 2005 IEEE International Conference on Pervasive Services.* Santorini. July 2005.

98. Md. Mafijul Islam and Per Stenstrom: Reduction of Energy Consumption in Processors by Early Detection and Bypassing of Trivial Operations. In *Proc. of the 6th IEEE Conference on Embedded Computer Systems: Architectures, Modelling, and Simulation (SAMOS VI)*. July 2006.

99. J.Jeong, P. Stenstrom and M. Dubois. Simple, Penalty-Sensitive Replacement Policies for Caches. In *Proc. of 2006 ACM Int. Conf. on Computing Frontiers.* May 2006.

100. H. Dybdahl and P. Stenstrom. Enhancing Lower Level Cache Performance by Early Miss Determination and Bypassing. In *Proc. of the 11th Asia-Pacific Computer Systems Architecture Conference (ACSAC06).* Shanghai, Sept 2006.

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102. M. Thuresson and P. Stenstrom. Scalable Value-Cache Based Compression Schemes for Multiprocessors. Accepted to *SBAC 2006*. October 2006.

103. H. Dybdahl, P. Stenstrom, L. Natvig, A Cache-Partition Aware Replacement Policy for Chip Multiprocessors. (Best Paper Award.) Accepted to *ACM 2006 HiPC*. December 2006.

104. Shekhar Y. Borkar, Norm Jouppi, Per Stenstrom. Microprocessors in the Era of Terascale Integration. Invited Paper. In *Proc. DATE 2007*. April 2007.

105. H. Dybdahl and P. Stenstrom. An Adaptive Shared/Private NUCA Cache Partiotioning Scheme for Chip Multiprocessors. In *Proc. of the IEEE HPCA 2007*. February 2007.

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107. Md. Mafijul Islam and Per Stenstrom. Energy and Performance Tradeoffs between Instruction Reuse and Trivial Computations for Embedded Applications. In *Proc. of the 2007 IEEE International Symposium on Embedded Computer Systems*. April 2007.

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116. M. Thuresson, M. Själander, P. Stenstrom. A Flexible Code-Compression Scheme using Partitioned Look-Up Tables. Submitted to *4th Int. Conf. on High-Performance and Embedded Architectures and Compilers*. January 2009.

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5.4 Workshop papers (refereed)

120. E. Belitskaja, V. Sidorenko, and P. Stenström: "Testing of Memory with Defects of Fixed Configuration," in *Second International Workshop on Algebraic and Combinatorial Coding Theory*, pp. 24-27, Leningrad, September 1990.

121. T. Lundqvist and P. Stenström: "Integrating Path and Timing Analysis using Instruction-Level Simulation Techniques," in *Proc. of ACM SIGPLAN Workshop on Languages, Compilers, and Tools for Embedded Systems.* June 1998.

122. J. Jalminger and P. Stenström "Boosting Energy-Efficiency of Off-Chip Caches using Selective Data Prefetching", in *Proc. of IEEE Workshop on Complexity-Effective Computer Design*, held in conjunction with ISCA-2000, June 2000.

123. P. Rundberg and P. Stenström: Low-Cost Thread-Level Data Dependence Speculation on Multiprocessors," in *4th Workshop on IEEE Multi-Threaded Execution, Architecture and Compilation (in conj. with Micro-33),* Dec 2000. (Received the Best Paper award.)

124. J. Hollmann, A. Ardö, and P. Stenström: "Empirical Observations regarding Predictability in User Access Behavior in a Distributed Digital Library System". In *Second International Workshop on Internet Computing and E-Commerce (ICEC'02),* April 2002.

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131. Ana Bosque, Pablo Ibanez, Viktor Vinals, Per Stenstrom, and Jose Maria Llaberia. Characterization of Apache web server with Specweb2005. In Proc. of 2007 *IEEE MEDEA* workshop (in conjunction with PACT 2007), September 2007.

132. M. M. Waliullah and P. Stenstrom. Intermediate Checkpointing with Conflicting Access Prediction in Transactional Memory Systems. In *Proc. of First MULTIPROG workshop* (in conjunction with the Third Int. Conf on HiPEAC). January 2008.

133. Alessandro Bardine, Pierfrancesco Foglia, Giacomo Gabrielli, Cosimo Antonio Prete and Per Stenstrom. A Micro-Architectural Power-Saving Technique for D-NUCA Caches. In *Proc. of 4th Workshop on Unique Chips and Systems (*in conjunction with 2008 IEEE ISPASS). April 2008.

134. Mafijul Md. Islam and Per Stenstrom. *Zero Loads: Canceling Load Requests by Tracking Zero Values.* In the IEEE MEDEA Workshop (In concjunction with PACT). October, 2008.

5.5 Book Chapters (refereed)

135. P. Stenström: "Shared-Memory Multiprocessors: A Cost-Effective Approach to High-Performance Computing," in *Parallel Computing: Paradigms and Applications,* Albert Zomaya (editor), ISBN: 1-85032-188-4 International Thomson Computer Press (London, U.K), 1996.

136. P. Stenström, E. Hagersten, D. Lilja, M. Martonosi, M. Venugopal: "Shared-Memory Multiprocessing: Current State and Future Directions.", in *Advances in Computers,* Marvin Zelkowitz (editor), Academic Press, Vol. 53, pages 2-46, 2000.

137. P. Stenstrom: "The Paradigm Shift to Multi-Cores: Opportunities and Challenges," in *The Future of Computing — essays in Memory of Stamatis Vassiliadis,"* Koen Bertels, Sorin Cotofana, Georgi Gayadjiev, Kees Goosens, Said Hamdioui, Ben Juurlink, Arjan van Genderen, Stephan Wong (eds), ISBN 978-90-807-957-3-0, 2007.

5.6 Newsletters (unrefereed)

138. M. Brorsson and P. Stenström: “Visualisation of Cache Coherence Bottlenecks in Shared-Memory Multiprocessor Applications,” in *NewsLetter of the Technical Committee on Computer Architecture*, No 3, pp. 32-36, 1993.

139. P. Stenström: “Conception de la memoire dans les multiprocesseurs a memorie partagee,” in *Calculateurs Paralleles*, Vol 6, No 3, pp. 83-136, 1994. Translated into French by Christine Rochange and Pascal Sainrat of Institute de Recherche en Informatique de Toulouse.

140. M. Karlsson and P. Stenström “Using Prefetching to Hide Lock Acquisition Latency in Distributed Virtual Shared Memory Systems,” in *NewsLetter of the Technical Committee on Computer Architecture*. March 1997.

141. P. Stenström and F. Dahlgren: "A Holistic Approach to Computer System Design Education based on System Simulation Techniques," in *NewsLetter of the Technical Committee on Computer Architecture*, pp. 48-50, February 1999.

5.7 Editorials

142. P. Stenström: “Scalable Shared-Memory Architectures: Introduction to Minitrack,” in *Proc. of 27th Hawaii International Conference on System Sciences*, pp. 520-521, January 1994.

143. P. Stenström and F. Dahlgren: “Applications for Shared-Memory Multiprocessors: Guest Editors’ Introduction, in *IEEE Computer*, December 1996.

144. P. Stenström: “Architectural Trends for Shared-Memory Multiprocessors,” in *Proc of 30th Hawaii International Conference on System Sciences*. January 1997.

145. P. Stenström and Patrice Quinton. “Parallel Computer Architecture and Image Processing,” in *Proc. of EUROPAR’97*, pp. 763-765, Aug. 1997

146. V. Milutinovic and P. Stenström “Opportunities and Challenges for Distributed Shared-Memory Multiprocessors. Guest Editors’ Introduction, *Proceedings of the IEEE*. Vol 87 No 3, pp 399-404, March 1999.

147. S. Muller, P. Stenström, M. Valero, and S. Vassiliadis: “Parallel Computer Architecture”, in *Proc. of EUROPAR’00,* Aug. 2000.

148. Proceedings of the 2003 ACM Conference on Langauges, Tools & Compilers for Embedded Computer Systems, editors Frank Mueller and Per Stenström. San Diego June 2003.

149. Proceedings of the 2004 IEEE/ACM Proceedings of the 31st International Symposium on Computer Architecture, editors Michel Dubois, Arndt Bode, and Per Stenström. Munich, June 2004.

150. F. Mueller and P. Stenstrom. Introduction to Special Issue on “Languages, Compilers, and Tools for Embedded Systems,” in *ACM Trans. on Embedded Computer Systems.* 2005.

151. B. Monien, G. Gao, H. Simon, P. Spirakis, P. Stenstrom. Introduction to Special Issue on “2004 International Parallel and Distributed Processing Symposium” in *Journal of Parallel and Distributed Computing*. 2005.

152. P. Stenstrom, M. O’Boyle, F. Bodin, M. Cintra, Sally A. McKee (eds). *Transactions on HiPEAC*, Vol 1. Springer Verlag, 2007

153. K. De Bosschere, D. Kaeli, P. Stenstrom, T. Ungerer, D. Whalley (eds). *Proceedings of the 2007 International Conference on HiPEAC.* Springer Verlag, January, 2007.

154. M. Dubois and P. Stenstrom (eds). *Proceedings of the 2007 ACM International Conference on Computing Frontiers.* May 2007.

155. P. Stenstrom, M. Dubios, M. Katevenis, and R. Gupta (eds). *Proceedings of the 2008 International Conference on HiPEAC.* Springer Verlag, January, 2008

156. J. Carter, A. Gonzalez, and P. Stenstrom (eds). *Proceedings of the 2008 IEEE International Symposium on High-Performance Computer Architecture.* February 2008.

157. A. Mei and P. Stenstrom (eds) *Proceedings of the 2009 IEEE International Parallel & Distributed Processing Sympoisium. May 2009.*

158. P. Stenstrom (eds). Transactions on High-Performance Architectures and Compilers. Vol 2, 2009.

5.8 Selected Tech. Reports

1. P. Stenström: "*MUMS Processing Element: Hardware Design,"* Technical Report, Department of Computer Engineering, Lund University, June 1987.
2. P. Stenström: "*MUMS Processing Element: Architecture Manual,"* Technical Report, Department of Computer Engineering, Lund University, June 1987.
3. P. Stenström: "*Sequentially Consistent, Packet-Switched, Multiprocessor Memory Systems,"* Technical Report, Department of Computer Engineering, Lund University, March 1990.
4. A. Gupta, T. Joe, and P. Stenström: "*Performance Limitations of Cache-Coherent NUMA and Hierarchical COMA Architectures and the Flat-COMA Solution,*" Technical Report CSL-TR-92-524, Computer Systems Laboratory, Stanford University, October 1992.
5. F. Pong, P. Stenström, M. Dubois, "*An Integrated Methodology for the Verification of Directory-Based Cache Protocols,*" USC Tech. report, November 1994.

5.9 Reprints in Tutorials

- The paper "A Survey of Cache Coherence Schemes for Multiprocessors," originally published in *IEEE Computer,* Vol 23, No 6, pp. 12-24, June 1990 has been reprinted in "The Cache Coherence Problem in Shared-Memory Multiprocessors: Hardware Solutions," IEEE Computer Society Press, M Tomasevic and V. Milutinovic, 1993.
- The paper "Comparative Performance Evaluation of Cache-Coherent NUMA and COMA Architectures," originally published in *Proc. of 19th Annual International Symposium on Computer Architecture*, pp. 80-91, May 1992 has been reprinted in "The Cache Coherence Problem in Shared-Memory Multiprocessors: Hardware Solutions," IEEE Computer Society Press, M Tomasevic and V. Milutinovic, 1993.
- The paper "Comparative Performance Evaluation of Cache-Coherent NUMA and COMA Architectures," originally published in *Proc. of 19th Annual International Symposium on Computer Architecture*, pp. 80-91, May 1992 has been reprinted in "Multiprocessor Performance Measurement and Evaluation," IEEE Computer Society Press, L Bhuyan and X. Zhang, 1995.

5.10 Other Documents

- Position document on trends in Computer Science for the Swedish Research Council, 2003

5.11 Patents (pending and approved)

- *Multiprocessorsystem för att minska effektförbrukningen hos logik i förbindelser med processorer i systemet.* Filed 16 November, 2001 (in Sweden); March 1, 2003 (in the U.S.). Approved April 6, 2004 (in Sweden). Published (20030115402) Co-inventors: Magnus Ekman and Fredrik Dahlgren.

- *Coherence message prediction mechanism and multiprocessing computer system employing the same.* Inventors: Jim Nilsson, Anders Landin, Per Stenstrom. Filed by Sun Microsystems to U.S. Patent Office, April 18, 2003. Approved Dec 6, 2005 as US Patent 6,973,547.
- *Cache Coherency Protocol Including Generic Transient States*. Filed by Sun Microsystems to U.S. Patent Office, Inventor: Per Stenstrom, March 2004. Published (20050210203). Approved March 22, 2008. US Patent 7,350,032
- *System and Method for Coherence Prediction.* Filed by Sun Microsystems to U.S. Patent Office. Inventor: Per Stenstrom. Filed May 2005. Approved April 24, 2008. U.S. Patent 7,363,435
- *Method and System for Process Memory Management.* Filed by Sun Microsystems to U.S. Patent Office, September 2004. Approved on September 8, 2009 as US Patent 7,587572. Inventor: Per Stenstrom.
- *Speculative Throughput Computing.* Filed as a utility patent by Nema Labs AB to U.S. Patent Office and PCT through European Patent Office, January 2008. Inventors: Alexander Busck, Mikael Engbom, Per Stenstrom, Fredrik Warg. Published July 31, 2008 at USPTO (20080184018, 20080184012, 2008014011)
- *A Robust Main Memory Compression Scheme*. Provisionally filed by Sun Microsystems, November 2004. Inventors: Magnus Ekman and Per Stenstrom
- *Multi-level Main Memory.* Filed by Sun Microsystems to U.S. Patent Office, Inventors: Robert Cypher, Andrew Phelps, Anders Landin, Magnus Ekman, and Per Stenstrom, March 2005.
- *Method and Mechanism for Cache Compaction and Bandwidth Reduction.* Filed by Sun Microsystems to U.S. Patent Office. Inventor: Per Stenstrom. Filed August 2005.
- *Dynamic Pointer Disambiguation.* Filed by Nema Labs AB to U.S. Patent Office and PCT through European Patent Office, July 2008. Inventors: Alexander Busck, Mikael Engbom, Per Stenstrom, Fredrik Warg.

6. Graduated Licentiate and Ph. D. Students

Ph. D. Theses

- Mats Brorsson: *"Performance Impact of Shared Memory Latency in Multiprocessors: Models and Experiments,"* Ph. D. thesis, Department of Computer Engineering, Lund University, May 1994. First employment Assist. prof. Lund Univeristy.
- Fredrik Dahlgren: *"Design and Performance Evaluation of Hardware-Based Cache Protocol Extensions for Multiprocessors,"* Ph. D. thesis, (main advisor) Department of Computer Engineering, Lund University, November 1994. First employment: Assist. res. prof. Lund University.
- Håkan Grahn: "*Evaluation of Design Alternatives for a Directory-Based Cache Coherence Protocol in Shared-Memory Multiprocessors,*" Ph. D. thesis, (main advisor) Department of Computer Engineering, Lund University, December 1995. First employment: Assist. prof. University of Karlskrona/Ronneby.

- Jonas Skeppstedt: "*Compiler Based Approaches to Reduce Memory Access Penalties in Cache-Coherent Multiprocessors,*" Ph. D. thesis (main advisor), Department of Computer Engineering, Chalmers University of Technology, May 1997. First employment: Assist. prof., Halmstad University.
- Magnus Karlsson: "*Data Prefetching Techniques Targeting Single and a Network of Processing Nodes*". Ph. D. thesis (main advisor), Department of Computer Engineering, Chalmers University of Technology, December 1999. First employment: Hewlett Packard Laboratories, Palo Alto.
- Ashley Saulsbury: "*Attacking Latency Bottlenecks in Distributed Shared Memory Systems,"* Ph.D. thesis (co-advised with Prof. Seif Haridi), Department of Teleinformatics, the Royal Institute of Technology, Stockholm, December 1999. First employment: Sun Microsystems, Menlo Park.
- Thomas Lundqvist: *"A WCET Analysis Method for Pipelined Microprocessors and Cache Memories"*, Ph. D. thesis (main advisor), Department of Computer Engineering, Chalmers University of Technology, June 2002. First employment: Lecturer at University College West.
- Jim Nilsson: "*Towards Accurate and Resource-Efficient Coherence Prediction*" Ph. D. thesis (main advisor), Department of Computer Engineering, Chalmers University of Techology, January 2004. First Employment: Startup company.
- Magnus Ekman: *"Strategies to Reduce Energy and Cost of Chip Multiprocessor Systems,"* Ph. D. thesis (main advisor), Department of Computer Engineering, Chalmers University of Techology, December 2004. First employment: Sun Microsystems.
- Fredrik Warg: "*Techniques to Reduce Thread-Level Speculation Overhead,"* Ph. D. thesis (main advisor), Department of Computer Engineering, Chalmers University of Techology, June 2006. First employment: Nema Labs.
- Martin Thuresson: "Compression Techniques for Improved Bandwidth and Static Code Size in Computer Systems". Department of Computer Engineering, Chalmers University of Techology, September 2008. First employment: Google.

Licentiate Theses (half-way between the MSc. and Ph. D. degree)

- Magnus Broberg: "*An Approach to Tune Performance of Multithreaded Programs on Multiprocessors,*" Licentiate thesis (examiner, main advisor: Lars Lundberg), Department of Computer Science, University of Karlskrona/Ronneby, June 1999.
- Ulf Assarsson: "*View Frustum Culling and Animated Ray Tracing: Improvements and Methodological Considerations"*, Licentiate thesis (main advisor, co-advised with Dr. Tomas Möller). May 2001.
- Jonas Jalminger. "*On Improving Data Cache Space Utilization*", Licentiate thesis (main advisor), Jan 2002.
- Martin Kampe. "*Prediction Methods for Cache and Branch Management in Computers,* Licentiate thesis (co-advised with Dr. Fredrik Dahlgren, and Prof. Michel Dubois), May 2002.
- Peter Rundberg. "*Data Dependence Speculation Methods to Expose Thread-Level Parallelism* (main advisor), Nov 2002.
- Jochen Hollman "*Latency Reduction and Tolerance in Distributed Digital Libraries*" (main advisor in collaboration with Dr. Anders Ardö) Sept 2003
- Md. Mafijul Islam. "*Improving Execution Efficiency by Targeting Redundancy and Parallelism"* (main advisor) November 2007

- M. M. Waliullah. *"Schemes for Improving the Efficiency of Hardware Transactional Memory"* (main advisor) January 2008
- Nima Namaki. *"Dominated Performance: Methodology, Tools and Empirical Experiments. (*co-advised with Stefan Christiernin), December 2008.

7. Professional Services

7.1 Editorial Services

- Editor-in-chief, Transactions on High-Performance Embedded Architectures and Compilers *Transactions on HiPEAC*, 2004-
- Editor of IEEE Transaction on Computers, between March 2000-2004
- Editor of IEEE Transactions on Parallel and Distributed Systems November 2008 - 2012.
- Editor (area: shared-memory multiprocessors) for JPDC (Journal of Parallel and Distributed Computing) since October 1993.
- Editor of the Journal of Universal Computer Science since 1994; one of the first electronic journals in the field.
- Editor of IEEE/TCCA *Computer Architecture Letters*, since December 2001.
- Editor of the *International journal of embedded systems*, since February 2004.
- Guest editor for "Applications for Shared-Memory Multiprocessors" in the December 1996 issue of IEEE Computer together with Dr. Fredrik Dahlgren.
- Guest editor for "Distributed Shared-Memory Multiprocessors" in the Spring issue 1999 of the Proceedings of the IEEE together with Dr. Veljko Milutinovic.
- Guest editor for "Languages, Compilers, and Tools for Embedded Systems" in ACM Transaction on Embedded Computer Systems in March, 2004 together with Dr. Frank Mueller.
- Guest editor for "Transactions on HiPEAC" top papers in 2005 International Conference on High-Performance Embedded Architectures and Compilers, March 2006.
- Guest editor for "Transactions on HiPEAC" top papers in 2007 International Conference on High-Performance Embedded Architectures and Compilers, March 2007.
- On the Editorial Committee for selecting the articles of the Dec 2004 issue of IEEE Micro Magazine on Top Picks in Computer Architecture.

7.2 Chairmanship & Steering Committee Appointments

- Minitrack coordinator for "Shared Memory Multiprocessors" in the 27th Hawaiian International Conference on System Sciences, 1994.
- Program vice-chair, 14th IEEE Symp. on Distributed Computer Systems, 1994
- Task force leader for "Trends in Shared-Memory Multiprocessing" in the 30th Hawaiian International Conference on System Sciences, 1997.
- Global chair for the Parallel Computer Archhitecture Topic of Euro-Par'96 and 2000.
- General chair for the 28th IEEE/ACM Annual International Symposium on Computer Architecture held Gothenburg, July 2-4,2001
- Program chair of ACM/SIGPLAN LCTES'2003 (Languages, Tools & Compilers for Embedded Systems).

- Program vice-chair of Architecture Track of 2004 IEEE International Parallel and Distributed Processing Symposium.
- Program chair of 31st IEEE/ACM Annual International Symposium on Computer Architecture held in Munich, 2004.
- Program vice-chair of the Architecture track of the 2004 ACM Conference on High-Performance Computing.
- Program track chair of the High-Performance Embedded Processor Architecture Track of the 2005 ACM Computing Frontier Conference.
- Program co-chair of 2007 High-Performance Embedded Architecture and Compiler Conference.
- Program co-chair of 2007 ACM Computing Frontiers Conference.
- General co-chair of 2008 High-Performance Embedded Architecture and Compiler Conference.
- Program vice-chair of Architecture Track of 2007 IEEE International Parallel and Distributed Processing Symposium.
- Program co-chair of the 14th IEEE International Symposium on High-Performance Computer Architecture 2008.
- Program chair of the 2009 IEEE International Parallel and Distributed Processing Symposium.
- Program vice-chair of the Computer Architecture and Real-Time Systems Track for the 2010 ACS/IEEE International Conference on Computer Systems and Applications, Tunisia, May 2010.
- Organizer and founder of the MULTIPROG Workshop held in conjunction with the HiPEAC conference series on January 27 in Göteborg for the first time and in Paphos, Cyprus in 2009 for the second time, and in Pisa, Italy in 2010 for the third time.
- Organizer of Barcelona Multi-core Workshop held in Barcelona June 5-6, 2008
- Member of the Advisory Board of the EUROPAR conference series, since 1995.
- Member of the IEEE TCCA Chair Nomination Committee 2001.
- Member of the advisory committee of IEEE CS TCCA (2001-2005)
- Member of Steering Committe of IEEE/ACM 28th, 29th, 31st, 32nd, and 33rd ISCA
- Member of Steering Committee of ACM/SIGPLAN LCTES (Languages, Tools & Compilers for Embedded Systems) since 2002.
- Member of Steering Committee of the Conf. on High-Performance Embedded Architectures and Compilation (since 2005).
- Member of the ACM/IEEE Eckert-Mauchly Award Committee 2004-2007.
- Steering Committee Chair for the International Conference on High-Performance and Embedded Architectures and Compilers series. 2007-
- Member of the ACM SIGARCH Distinguished Service Award Committee 2008-2010 and chairman for it in 2010.

7.3 Program Committe Membership

- **IEEE conferences:** 13th ICDCS, 1993, (member); 2nd, 3rd, 6th, 7th, 8th, 12th, 14th HPCA, 1996, 1997, 2000, 2001, 2002, 2006, 2008 (member); 23rd, 24th, 27th, 30th, 31st, 33rd, and 37th ISCA (co-sponsored by ACM), 1996, 1997, 2000, 2003 (mem-

ber), 2004 (chair), and 2006 (member), 2010 (member). 8th SPDP (1996), IPDPS (2003, 2004, 2006, 2007), 37th, 38th Micro (co-sponsored by ACM) 2004, 2005, PACT (2004,2007,2009), ISPASS (2005,2006).

- **ACM conferences:** 7th, 9th, 15th ASPLOS, 1996, 2000, 2006 (member), SC'97, ICS'98, ICS'03, ICS'04, ICS'05. HiPC'96, HiPC'98, HiPC'03 (member) HiPC'04 (co-chair), HiPC'05 (member), LCTES'03 (chair), LCTES'06 (member), Computing Frontier CF'05 (track chair) CF'07 (program chair)
- **Other conferences:** Euro-Par 95 (member), Euro-Par 97 (global chair for topic), Euro-Par 99 (vice-chair for topic), Euro-Par 00 (global chair for topic), PDCS'97-99, ICPP'98, ICPP'99, ICPP-2001, and ICPP-2002. HIPEAC 2005, 2007 (chair), HiPEAC 2009. DATE 2006, DATE 2007. SSS 2009 (International Conference on Stabilization, Safety, and Security of Distributed Systems).
- **Workshops:** CANPC'97 and CANPC'98, EWOMP'99, IEEE Memory Wall workshop (in conjunction with ISCA 2000), MEDEA workshop in conjunction with PACT 2000, 2006, 2007, and 2009. EASY workshop in conjunction with ISCA-2001. MTEAC-6 in conj. with MICRO-35, 2002. dasCMP 2005, dasCMP 2006, dasCMP 2007, dasCMP 2008. MULTIPROG 2008 and 2009 (in conj. with HiPEAC) WRC 2008 and 2009 (in conj. with HiPEAC)

7.4 Reviewing for Scientific Conferences, Journals & Textbooks

- Referee for IEEE Computer, IEEE Micro, IEEE Concurrency, Journal of Parallel and Distributed Computing, IEEE Transactions on Computers, IEEE Transactions on Parallel and Distributed Systems, Proceedings of the IEEE, ACM Transactions on Computer Systems, Parallel Computing, IEE Proceedings, Journal of Microprocessors and Microsystems, Journal of Universal Computer Science, Journal of Real-Time Systems, ACM Transactions on Embedded Computer Systems, IEEE/ACM International Symposium on Computer Architecture (ISCA), International Conference on Parallel Processing (ICPP), ACM Supercomputing, IEEE International Conference on Distributed Computing Systems, IEEE International Parallel Processing Symposium (IPPS), IEEE International Symposium on Parallel and Distributed Systems, IEEE International Symposium on High-Performance Computer Architecture (HPCA), ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), Euro-Par, Hawaii International Conference on System Sciences, Parallel Architectures and Compilation Techniques (PACT), ACM International Conference on Supercomputing (ICS) ACM Principles of Programming Languages (POPL), International Conference on High-Performance Embedded Architectures and Compilers, Transactions on High-Performance Embedded Architectures and Compilers, and others.
- Review of textbook proposals for Addison-Wesley, Morgan Kaufmann (1997 and 2001), Cambridge University Press, and tutorials for IEEE Computer Society Press.

7.5 Reviewing of Grant Proposals & Applicants for Academic Positions

- Review of research grant proposals for the National Science Foundation (NSF) (1991,1997), the Swedish Research Council for Engineering Science (TFR) (1995), the Swedish Foundation for Strategic Research (1998-1999), and the Norwegian Science Foundation (NFR) (1996-2000), chair of evaluation panel in CS for Swedish Research Council 2001-2004. On the evaluation panel on the priority program on Organic Computing for the German Science Council (DFG), February 2005. On the panel to evaluate prolongation of research programs in CS for SSF, December-January 2005/2006.

- Expert evaluations of applicants for associate professorships in computer science and engineering at Kristianstad University College (1993), Lund University (1994), Karlskrona/Ronneby University (1995,1999), Chalmers University of Technology (1994, 1997), Royal Institute of Technology (1997, 1998, 2000), Luleå University (1998, 2000), Kuwait University (1998), Uppsala University (1999, 2002), Trollhättan (2003). Malardalen (docent) 2005, 2008, University of Cyprus (2006).
- Evaluations for promotion to assistant/associate professor (U.S.A.): Rice university (1998), Cornell University (1998), Princeton University (1999), Rochester Univ. (2001), Rutgers University (2002, 2003), University of Maryland (2003). University of Illinois - Urbana Champaign. (2004), University of Massachusetts, Amherst (2005)., Harvard (2009).
- Evaluations for promotion to Reader at Imperial College (U.K.) (2001), Full professor promotion University of Edinburgh (2005), Reader, Edinburgh (2009).
- Evaluations for promotion to full professor (U.S.A): University of Minnesota (1999), Georgia Institute of Technology (1999), Rice University (1999), University of Texas at Austin (2000), University of Southern California (2003), University of California, San Diego (2003), Northeastern University (2004), Rochester (2006), CMU (2006), University of Colorado (2008).
- Expert evaluations of applicants for full professorships at Luleå Technical University (1996, 2004), the University of Mälardalen (1997,1998, 2001), Karlskrona/Ronneby University (1998), Uppsala (1999), Royal Institute of Technology (2000,2003), and Jönköping University (2002), Denmark Technical University (2005).
- Member of group to establish criteria for applications for promotions to full professors at Uppsala University and Umeå University (1999).
- Member of the National Committee for promotion to full professsor in Computer Science (1999)
- Reviewer and member of evaluation committees of Ph. D. theses at Royal Institute of Technology (1992,1997,1998,2004), Uppsala University (1994,1997,2000, 2002,2006 x3), Chalmers University of Technology (1994,1998,2001,2006), Oslo University (1998), Joensuu University, Finland (1998), University of Paris Sud (2002,2005), Luleå University of Technology (2000, 2004). IT-university, Göteborg (2004, 2006), Blekinge Institute of Technology (2005), TU Delft (2006), University of Edinburgh (2008).
- Jury member at Dr. Pascal Sainrat's habilitation dissertation at University of Paul Sabbatier and Institute de Recherche en Informatique de Toulouse, March 1998.
- Jury member and referee of Stephane Louise's Ph. D. thesis at University of Paris Sud. Jan 2002.
- Jury Member of the Ph.D dissertation of Christian Fench (Edinburgh, 2008).
- Jury Member of the Ph. D. dissertation (Manchester 2009).
- Faculty opponent at Knut Omang's thesis defense at University of Oslo in June 1998.
- Faculty opponent at Uppsala University, May 25, 2000, for Mikael Sjödin.
- Member of a committee to define the scope of a new EU-IST program on "Emerging Computing Architectures: New Processor Architectures and Advanced Compiler Technologies" in the spring of 2004.
- Recipient of a certificate of belonging to the category of best senior reviewers for IEEE Computer in 1994.
- PhD Jury member INRIA/University Paris Sud Daniel Gracia Perez, October 2005.

7.6 Other Professional Activities

- Moderator on a panel of the 3rd IEEE workshop on Scalable Shared-Memory Multiprocessors in San Diego, May 1993.
- Moderator on a panel on the 5th IEEE workshop on Scalable Shared-Memory Multiprocessors in Santa Margherita Ligure, Italy, 1995.
- Organized a task force on “Architectural Trends for Shared-Memory Multiprocessors” in conjunction with HICSS’97 Wailea, Hawaii.
- Panelist at the IEEE workshop CANPC’98 in conjunction with HPCA’98
- Panelist at the IEEE workshop CAECW’2000 in conjunction with HPCA’2000
- Organized a panel at the Sixth Swedish Workshop on Computer Systems Architecture, Gothenburg, May 1998.
- Organized a panel at IPDPS 2007 on Multi-core issues.

7.7 University Services

- Was an expert in the procurement committee of a supercomputer platform at Chalmers to service computational scientific problems in virtually all disciplines at Chalmers (1996-1997)
- Participated in the development of D++, a new education program in Computer Science and Engineering. Specifically, I designed a specialization in Computer Systems (1995-1999).
- I acted as a chair of the council for the faculty of the School of Electrical Engineering and Computer Science (1998-1999).
- I was part of a working group to review Forskning 2000, a governmental evaluation of the research policy for the next decade (1999).
- I was vice-dean of the School of Electrical and Computer Engineering with responsibility of the Ph. D. Education between 1999-2002.
- I was vice-dean of the School of Computer Science and Engineering with responsibility of the Ph. D. Education between 2002-2003.
- I was member of the faculty council between 1999 and 2002.
- I was part of a working group to provide the government with input for strategic research actions, Dec 1999.
- I was a member of the recruitment committee at the School of EEC and M&CS from May 2000 and Jan 2001, resp. until 2002. Between 2002 until 2005, I held the same position in the school of CSE.
- I was the chair of the recruitment committee at the IT University of Goteborg between 2002-2005 and continued to serve this committee until 2007.
- I was the chair of the research committee at the School of Electrical and Computer Engineering, from June 2000 until 2002.
- I was on the steering committee for the planning of the IT-University in Goteborg between 2000 and until a permanent organization was formed in 2002.
- I was on the admission committee for selecting 3rd-grade students at the engineering programs for studies at foreign partnership universities (2001-2003)
- I was on the steering committee for student recruitment strategies at Chalmers, 2001-2002.

- I am leading the departmental recruitment group to be responsible for the process of recruiting (non-tenured) assistant professors to the department.

8. International Talks and Lecture

I have delivered more than a hundred research presentations over the years; a majority of them internationally.

- Carnegie-Mellon University, Pittsburgh, U.S, Oct. 1986.
- IBM Yorktown Heights, New York, U.S., Oct. 1986.
- PARLE conference, Eindhoven, Holland, June 1987.
- “A Cactus Stack Multiprocessor Memory Organization” HICSS’21 conference, Hawaii, U.S., Jan. 1988.
- N.E.C. corporation, Kawasaki, Japan, Dec. 1988.
- International seminar on performance of distributed and parallel systems, Kyoto, Japan, Dec. 1988.
- 16th ISCA, Jerusalem, Israel, June 1989.
- Hebrew University, Jerusalem, Israel, Jan. 1990.
- University of Washington, Seattle, U.S., Sept. 1990.
- Ready Systems Inc., Sunnyvale, U.S., Sept. 1990.
- U. C. Berkeley, Berkeley, U.S., Sept. 1990.
- Stanford University, Stanford, U.S., Sept. 1990.
- International Computer Science Institute (ICSI), Berkeley, U.S., Sept. 1990.
- University of Southern California, Los Angeles, U.S., Sept. 1990.
- Dolphin Server Technology A/S, Oslo, Norway, Nov. 1990.
- Oslo University, Oslo, Norway, Nov. 1990.
- University of Edinburgh, Edinburgh, U.K., May 1991.
- Stanford University, Stanford, U.S., June 1991.
- Intel Corporation, Santa Clara, U.S., Dec. 1991.
- 20th International Conference on Parallel Processing, Chicago, 1991.
- University of Southern California, Los Angeles, U.S., Dec. 1991.
- International Parallel Processing Symposium, Los Angeles, U.S., March 1992.
- 19th ISCA, Gold Coast, Australia, May 1992.
- Stanford University, Stanford, U.S., Jan. 1993.
- M.I.T., Cambridge, U.S., Jan. 1993.
- New York University, New York, U.S., Jan. 1993.
- ICSEE’93 conference, San Diego, Jan. 1993.
- University of Southern California, Los Angeles, U.S., Jan. 1993.
- 3rd Workshop on Scalable Shared-Memory Multiprocessors, San Diego, U.S., May 1993. Moderator on a panel.
- University of Michigan, Ann Arbor, U.S., April 1994.

- 4th Workshop on Scalable Shared-Memory Multiprocessors, Chicago, U.S., May 1994.
- G.M.D., Berlin, Germany, June 1994.
- Ecole d'ete des jeunes chercheurs (summer school), Toulouse, France, July 1994. (Invited)
- University of Southern California, Los Angeles, U.S., January 1995.
- Stanford University, Stanford, U.S., January 1995.
- Tech talk at Sun Microsystems, Menlo Park, U.S., January 1995. (Invited)
- 5th Workshop on Scalable Shared-Memory Multiprocessors, Santa Margherita Ligure, Italy, June 1995.
- University of Washington, Seattle, U.S, Sept. 1995 (Colloquim, invited)
- University of Southern California, L.A., U.S, Sept 1995
- Digital Equipment Corporation WRL, Palo Alto, U.S. Sept 1995.
- University of Pisa, Feb. 1996.
- Hawaii International Conference on System Sciences, Wailea, Maui, Jan. 1997
- Gave a tutorial at EUROPAR'97, Aug. 1997, in Passau, Germany (Invited)
- Invited talk at EUROPAR'97, Aug. 1997 in Passau, Germany
- Invited talk at INFOFEST'97 in Montenegro, Jugoslavia, Sept. 1997.
- Panelist at CANPC'98 in conjunction with HPCA'98, Las Vegas, Feb. 1998 (Invited).
- Gave a tutorial at Technical University of Catalunya, Barcelona, Spain, Feb 1998. (invited)
- Universitet Paul Sabatier (and IRIT), Toulouse, France, March 1998.
- Ericsson Research, Älvsjö, April 1998.
- 1998 IEEE Workshop on Computer Architecture Education in conjunction with 25th ISCA in Barcelona, June 1998. (Invited)
- ARTES Summer school, Lidingö Stockholm, Aug. 1998. (invited)
- Sun Microsystems, Menlo Park, CA, Sept. 1998.
- Research overview at the Winter Meeting for CS Dept., Chalmers, Smögen, Jan 1999
- Thread-Level Data Speculation Techniques, Ericsson Research, Älvsjö, April 12, 1999
- All-Software Thread-Level Data Speculation Systems, Dagstuhl Seminars, April 21, 1999 (Invited)
- Polytechnic University of Barcelona, "On the Interaction between Commerical Workloads and Memory Systems in High-Performance Servers," Sept 9, 1999.
- University of Maryland, "On the Interaction between Commerical Workloads and Memory Systems in High-Performance Servers," Colloquim, Invited talk, Sept 16 1999.
- University of Southern California, "On the Interaction between Commerical Workloads and Memory Systems in High-Performance Servers," Sept 20, 1999.
- Princeton University, "On the Interaction between Commerical Workloads and Memory Systems in High-Performance Servers," Sept 22, 1999.
- Panelist at CAECW at HPCA-6 in Toulouse, January 9, 2000.

- ETH, Switzerland, Colloquium, June 8, 2000 “Access Latency Reduction and Hiding Techniques for High-Performance Computers”. (Invited)
- ETH, Switzerland, June 9, 2000 “Boosting Energy-Efficiency for Off-Chip Caches using Small Block Sizes and Selective Prefetching”.
- Imsys AB, Stockholm, Aug 7, 2000 “Challenges in Computer Architecture”
- “Understanding Performance Bottlenecks in Complex Computer Systems” (invited talk), First Summer school on Engineering of Complex Computer Systems, Skövde University, Aug. 15., 2000.
- Metoder för effektivt utnyttjande av multiprocessorteknologi i transaktionsorienterade system: Project presentation at the NUTEK program conference, Lund, Sept. 11, 2000.
- Opening address at IEEE/ACM Int Symp. on Computer Architecture (ISCA-2001) July 2, 2001 in Gothenburg.
- “Can We ever Dream of Making Multiple Processors and Caches Appear as a Simple and Single Entity to the Software” Keynote speech at ICPP-01 on Sept 7, 2001. Valencia, Spain. (Invited)
- “All-Software Thread-Level Data Speculation on Multiprocessors” Invited talk at University of Paris-Sud XI, Jan 21, 2002.
- Lecture series in Parallel Computer Architecture. Technical University of Calatonia, Barcelona. April 2002. (Invited)
- Keynote Talk at IPDPS-2003 (Invited)
- Distinguished Lecture Talk at University of Southern California, January, 2003 (Invited)
- Several talks at Sun Microsystems during spring 2003 during my sabbatical there.
- Colloquim at University of Texas, Austin, April 7, 2003. (Invited)
- NSF Panel, June 2003 (Invited).
- IT-University, Göteborg, Sept and Oct 2003
- Lund University, Nov. 2003
- Keynote speech at ACM HiPC’2003 in Hyderabad (India), December 20, 2003 (Invited)
- Sun Microsystems, Feb 9, 2004
- Computing Frontier conference, Ischia, Italy, April 15, 2004 (Invited)
- Opening Address at 31st International Symp. on Computer Architecture, Munich, June 2004.
- Sun Microsystems, August 9, 2004
- “A Robust Memory Compression Scheme” (Invited) University of Illinois Urbana-Champaign, December 2004.
- ACACES 2005. Summer school arranged by HiPEAC on Chip-multiprocessors. July 2005, Italy. (Invited)
- Sun Microsystems, Nov 2, 2005.
- Keynote speech at the First HiPEAC conference, Barcelona, Nov. 18, 2005. (Invited)
- Keynote speech at 12th IEEE Symposium on High-Performance Computer Architecture, Feb 14, 2006, Austin Texas.

- Sun Microsystems, Feb 16, 2006.
- Multi-core Expo, Munich, Nov 16-17, 2006, invited talk
- EU FP7 conference, invited talk at session on Computing Systems, Nov 21-22, 2006, Helsinki
- Moderated a panel on Multi-core challenges at IPDPS 2007.
- Invited talk at DATE on future of computer architecture, April 17, 2007.
- Invited talk at Google, Trondheim, Norway, May 3, 2007
- Invited talk at Ericsson AB, May 24, 2007
- Invited talk at BSC/UPC Barcelona, July 31, 2007
- Invited talk at Stamatis Vassiliadis Symposium, Delft, Sept 28, 2007
- Talk at FET ICT Consultation workshop on "Massive ICT Systems", Brussels, November 7, 2007.
- Talk at EU IST FP7 Consultation workshop on "High-Performance Computing Systems", Brussels, Dec 17., 2007.
- Invited talk at University of Edinburgh, May 12, 2008.
- Invited talk at the Barcelona Multicore Workshop, June 5, 2008
- Panelist on a panel arranged by Yale Patt at the Barcelona Multicore Workshop, June 5, 2008
- HiPEAC presentation at EU meeting in Seoul Korea, June 16, 2008 (invited)
- Keynote presentation at ISCA workshop, June 21, 2008, Beijing, China.(invited)
- Presentation at Multicore Days Stockholm September 11-12, 2008
- Panelist at Multicore Days, Stockholm Sept. 11-12, 2008
- Talk in Lund on October 17.2008
- Presentation at "Multicores: Theory and Practice" in the EU project ACTORS at Technical University of Kaiserslautern, Germany October 28, 2008
- Panelist at the SMART 2009 workshop held in conj. with 4th Int. Conf on HiPEAC, Cyprus 2009.
- Panelist at the 2009 International Parallel & Distributed Processing Symposium.
- Gave a talk at Multicore Day in Kista on September 15, 2009 on how to use Nema Labs technolgy to accelerate making the code multicore ready.
- Gave a talk at SC 2009 on FASThread technology. Nov 2009
- Gave a talk at University of Washington on FASThread technology. Nov 2009

9. Awarded Research Grants

9.1 Research projects (grants)

The first name corresponds to the P.I.

- Lars Philipson and Per Stenström: *Laboratory of Experimental Computer Architecture*, 1990-1993, STU, about 2.4 MSEK
- Lars Philipson and Per Stenström*: Laboratory of Experimental Computer Architecture*, 1993-1996, NUTEK, about 1.8 MSEK.
- Per Stenström: *Scheduling of Memory Instructions for Shared-Memory Programs*, 1994-1997, TFR, about 1 MSEK

- Per Stenström and Per Andersson: *ATM-based Multiprocessor Interconnects*, 1994-1996, NUTEK, about 800 KSEK.
- Per Stenström: *Performance Prediction Testbed for Mobile Packet Data Applications*, 1996-1997, NUTEK. about 700 KSEK
- Per Stenström: *Methodologies and techniques to estimate worst-case execution time*. 1997-2002. TFR, about 1.8 MSEK.
- Per Stenström, Bengt Nordström, and Mats Viberg: Equipment grant from FRN, about 3,5 MSEK, 1997-2000.
- Per Stenström: *A New Approach to Memory Hierarchy Management in Shared-Memory Multiprocessors*. TFR/SSF, about 1.5 MSEK, 1998-2001
- Per Stenström: Donation of an E4000 multiprocessor server from Sun Microsystems. About 1 MSEK
- Per Stenström. Collaborative Research on Multiprocessors for Database systems. CR with Sun Microsystems. $50,000 from Sun Microsystems. 1998-2000.
- Per Stenström, *Design Strategies for High-Performance Real-time Multimedia Applications on Shared-Memory Multiprocessors*, SSF, about 3 MSEK 1999-2003.
- Per Stenström: *A New approach to Thread-level Data Speculation Execution Models.* TFR, about 1 MSEK, 1999-2001.
- Per Stenström, "*Metoder för effektivt utnyttjande av multiprocessorteknologi i transaktionsorienterade system*, NUTEK about 700 KSEK, 2000.
- Per Stenström and Anders Ardö "*Networked implementation of a distributed electronic journal collection and full text archive*, NORDUNET-II, about 1 MSEK 2000-2001.
- Per Stenström (PI): "*Techniques for Module-Level Speculative Parallelization on Shared-Memory Multiprocessors*, SSF, 720 KSEK, 2000-2001
- Per Stenström (primary PI, together with Dr. Fredrik Dahlgren, Ericsson), *Support for Real-Time Grahpics 3D Graphics for Future Mobile Terminals under Energy/Area Constraints*. SSF, 1.2 MSEK 2000-2004.
- Per Stenström and Michel Dubois: *MECCA: Meeting the Challenges in Computer Architecture*, collaboration grant 500 KSEK/year for 2001-2004 from STINT.
- Pet Stenström. Methods for Adapting the Resource Demands in Computer Architectures under various Demand Objectives. Vetenskapsrådet, 1.8 MSEK, 2003-2006.
- Per Stenström (primary P.I.) FlexSoC: A Flexible Platform for System-on-Chip in Embedded Systems. SSF 10 MSEK, 2003-2007.
- Per Stenstrom (sole PI): Swedish Research Council 2004-2005. 1 MSEK.
- Per Stenström (Mateo Valero coordinator). *HiPEAC: High-Performance Embedded Architectures and Compilation Methods.*. EU Network of Excellence in Computer Architecture. 2004-2007. Leading a major effort as workpackage leader
- Per Stenstrom. *Compute Resources to Analyze Future Computer Architectures*. Admission to use the compute resources of SNIC.(2005-2006)
- Per Stenström (Stamatis Vassiliadis coordinator). *SARC: Scalable Computer Architecture.* EU Integrated project. 2005-2009. 6 MSEK. Leading a major effort as workpackage leader
- Per Stenström (Mateo Valero coordinator). VELOX - A STREP accepted by EU FP7. About 200 000 EU (2008-2010)

- Per Stenström (Koen De Bosschere coordinator). HiPEAC-2 Network of Excellence accepted by EU FP7. About 360 000 EU (2008 - 2011). Leading a major effort as workpackage leader
- Per Stenström (sole P.I.) Out-of-Order Thread Speculation. Swedish Research Council (2009 - 2012). 1.5 MSEK.
- Per Stenstrom (and as co-PIs Lars Svensson, Sally McKee, Per Larsson-Edefors) CHAMPP. Funded by the Swedish Research Councils with a budget of 3 MSEK (30000 Euro per year) from 2010 - 2014.

9.2 Awards and Honors

Awarded the grade of IEEE Fellow in 2007 and ACM Fellow in 2008. In 2009 I became a member of the Royal Swedish Academy of Engineering Sciences.

- Member of ACM SIGARCH and IEEE TCCA
- Biographical entry in The Marquis Who's Who in the World in the 12th-19th, 24th (2006) editions
- Biographical entry in Men of Achievement, the 17th edition (1996)
- Biographical entry in The Marquis Who's Who in Finance and Industry (2001)
- Biographical entry in The Marquis Who's Who in Science and Engineering (2006-2007)
- Became listed on the "IEEE/ACM ISCA Hall of Fame" signifying more than eight ISCA papers over the years (2005).
- Fellow of the IEEE in 2007.
- Fellow of the ACM in 2008.
- Member of the Royal Swedish Academy of Engineering Sciences in March 2009.

Best paper awards:

[1] H. Nilsson and P. Stenstrom: "An Adaptive Update-Based Cache Coherence Protocol for Reduction of Miss Rate and Traffic," *in Proc. of PARLE (Parallel Architectures and Languages Europe)*, pp. 363-374, June 1994. Best Paper Award at the conference.

[2] P. Rundberg and P. Stenstrom: Low-Cost Thread-Level Data Dependence Speculation on Multiprocessors," in *4th Workshop on IEEE Multi-Threaded Execution, Architecture and Compilation (in conj. with Micro-33)*, Dec 2000. (Received the Best Paper award.)

[3] H. Dybdahl, P. Stenstrom, L. Natvig, A Cache-Partition Aware Replacement Policy for Chip Multiprocessors. (Best Paper Award.) Accepted to *ACM 2006 HiPC*. December 2006.

[4] F. Warg and P. Stenstrom. Dual-Thread Speculation. Two Threads in the Machine is Better than Eight in the Bush. Accepted to *SBAC 2006*. (Best Paper Award) October 2006