

Luca Benini – List of Publications

Peer-Reviewed International Journals:

1. L. Benini, P. Siegel, G. De Micheli. **Saving power by synthesizing gated clocks for sequential circuits.** IEEE DESIGN & TEST OF COMPUTERS, vol. 11, no. 4, pp. 32–40, 1994
2. L. Benini, G. De Micheli. **State assignment for low-power dissipation.** IEEE JOURNAL OF SOLID STATE CIRCUITS, vol. 30, no. 3, pp. 258–268, 1995
3. L. Benini, G. De Micheli. **Automatic synthesis of low-power gated-clock Finite-State Machines.** IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, vol. 15, no. 6, pp. 630–643, 1996
4. L. Benini, P. Vuillod, A. Bogliolo, G. De Micheli. **Clock-skew optimization for peak current reduction.** KLUWER JOURNAL OF VLSI SIGNAL PROCESSING, vol. 16, no. 2/3, pp. 117–130, 1997
5. L. Benini, G. De Micheli. **A survey of Boolean matching techniques for library binding.** ACM TRANSACTIONS ON DESIGN AUTOMATION OF ELECTRONIC SYSTEMS, vol. 2, no. 3, pp. 193–226, 1997
6. A. Bogliolo, L. Benini, G. De Micheli, B. Riccò. **Gate-Level power and current estimation of Cell-Based CMOS Circuits.** IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS, vol. 5, no. 4, pp. 473–488, 1997
7. L. Benini, A. Bogliolo, G. De Micheli. **Regression models for behavioural power estimation.** INTEGRATED COMPUTER-AIDED ENGINEERING, vol. 5, no. 2, pp. 95–106, 1998
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11. A. Bogliolo, L. Benini, **Robust power macro-models,** IEEE TRANSACTIONS ON VERY LARGE-SCALE INTEGRATION SYSTEMS, vol. 6, no. 4, pp. 554–562, Dec. 1998.
12. H. Kapadia, L. Benini, G. De Micheli, **Reducing switching activity on datapath busses with control-signal gating,** IEEE JOURNAL OF SOLID-STATE CIRCUITS, vol. 34, no. 3, pp. 404–414, March 1999.
13. L. Benini, A. Bogliolo, G. Paleologo, G. De Micheli, **Policy Optimization for Dynamic Power Management,** IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, vol. 18, no. 6, pp. 813–833, June 1999.
14. L. Benini, G. De Micheli, A. Macii, E. Macii, M. Poncino, **Automatic selection of instruction op-codes of Low-Power Core Processors,** IEE PROCEEDINGS. COMPUTERS AND DIGITAL TECHNIQUES, vol. 146, no. 4, pp. 173–178, July 1999.

15. L. Benini, G. De Micheli, A. Lioy, E. Macii, G. Odasso, M. Poncino, **Automatic Synthesis of Large Telescopic Units Based on Near-Minimum Timed Supersampling**, IEEE TRANSACTIONS ON COMPUTERS, vol. 48, no. 8, pp. 769–779, August 1999.
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28. L. Benini, E. Macii, G. De Micheli, **Designing Low-Power Circuits: Practical Recipes**, IEEE CIRCUITS AND SYSTEMS MAGAZINE, vol. 1, no. 1, pp. 7–25, Q1 2001.
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